Hardware implementation of a multi-channel EEG lossless compression algorithm

Federico Favaro, Juan Pablo Olvier

Facultad de Ingeniería
Universidad de la República

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Summary

- Wearable Electroencephalography (EEG):
  - Applications
  - Challenges
  - Data compression
- Motivations.
- Hardware implementation of the algorithm.
- Results: implemented circuit and algorithm performance.
- Future work.

Wearable EEG

- Wearable: wireless, low weight, and small size.
  - Low-power operation and energy-efficient wireless data transmission.

EEG Applications

- Applications:
  - Epilepsy: Seizure detection
  - Sleeping, mental disorders (depression).
  - Brain-Computer Interfaces: Non-invasive neuroprosthetics, wheelchair control.
  - Non-Medical: education&training, gaming, assisted driving.
- Some require high sampling rates. Example:
  - (64 ch) x (16 bits) x (2 kHz Sampling freq.) = 2 Mbps

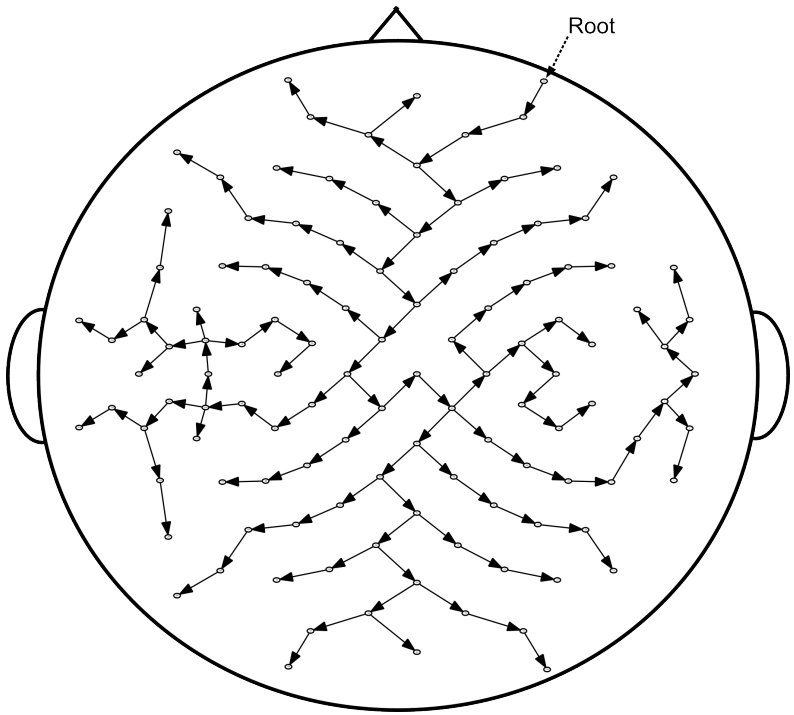
Data Compression

- How to reduce throughput? Data compression.
  - Drawback: Adds processing to the system.
- Trade-off: Power of wireless transmission vs. Power of data processing.
- Motivations:
  - Low complexity lossless and near-lossless compression algorithm [1].
    - Competitive compression ratios.
    - Highly efficient (fast, low resources required).
  - Tested in MSP432 (32-bit ARM Cortex-M4F):
    - Low Power consumption.
    - Limited throughput: Aprox 512 kbps

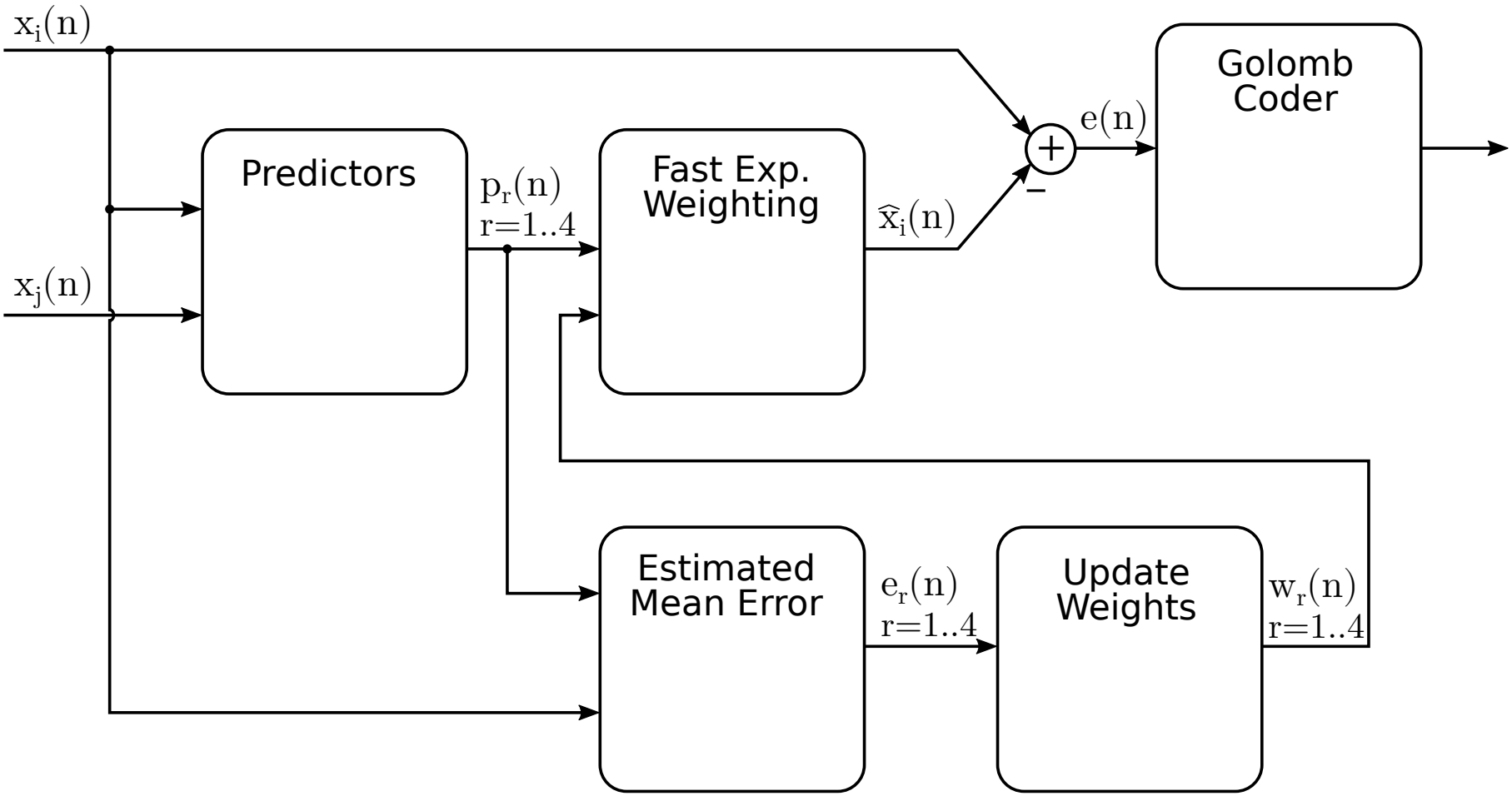
[1] **G. D. y. Álvarez, et al.**, "Wireless EEG system achieving high throughput and reduced energy consumption through lossless and near-lossless compression," *IEEE Transactions on Biomedical Circuits and Systems*.

Compression Algorithm

- Handles any number of channels:
  - Tree structure.
- Predictive stage followed by a coding stage.
- Prediction based on temporal and spatial correlation of EEG signals.
- Option for near-lossless encoding with controlled per sample distortion.



Implemented circuit



Implemented circuit

- Full-parallel approach: Compression of all channels simultaneously.
  - Fastest solution
  - Worst in terms of area and power
- Generic VHDL.
- Highly parametric design:
  - Bits per sample
  - Number of channels
  - Algorithm related parameters (affects compression).
- Signed Integers arithmetic.
- Data path precision: Adapts to input samples.

Results

- Tested on Cyclone V FPGA (5CEBA5F23C7).
- Tools: Quartus Prime 17.1.
- Setup: 21 channels, 16 bits per channel.
- Clock Frequency: 50MHz.
- Validated using simulations (Modelsim).
- Input samples: BCI Competition III.
  - Subset of 21 channels (10-20 Standard)
  - Down-sampled to 500 Hz.

Results

Resource utilization per channel:

ALUTs	Registers
1921	840

- For 21 channels is 85% of 5CEBA5F23C7 device.

Algorithm results:

Compression Ratio	Compression Time Per Sample	Max Sampling Rate
2.7	0.52 us	1.9 Mbps

- Average CTPS of slowest channel.

Power consumption:

Per Channel	Total
10 mW	215 mW

- Estimated using Power Play Analyzer.

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Algorithm results:

Compression Ratio	Compression Time Per Sample	Max Sampling Rate	SR μC
2.7	0.52 us	**1.9 Mbps**	**3.5 ksps**

- Average CTPS of slowest channel.

Power consumption:

Per Channel	Total	μC Power
10 mW	**215 mW**	**6.4 mW**

- Estimated using Power Play Analyzer.

Low power architecture

- Preliminary results. Need to reduce power consumption.
- There is room for reducing power consumption by switching to an architecture that re-uses resources. (Less area: smaller device)
- Compression speed allows sampling rates that exceeds requirements by far.

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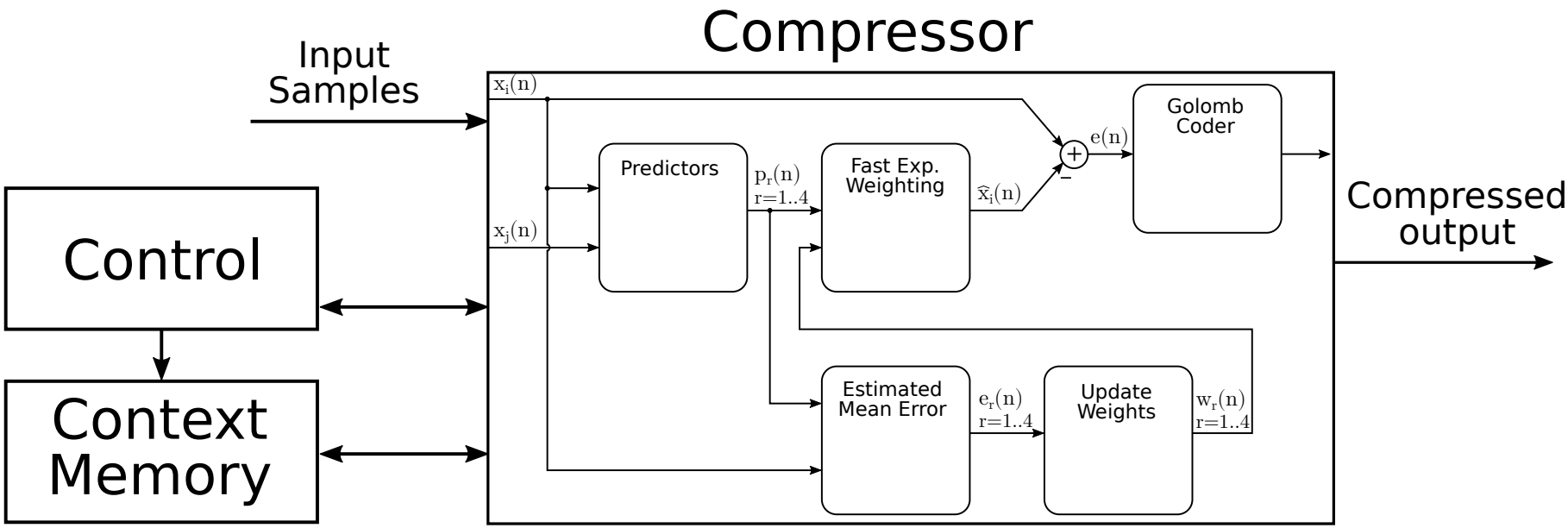
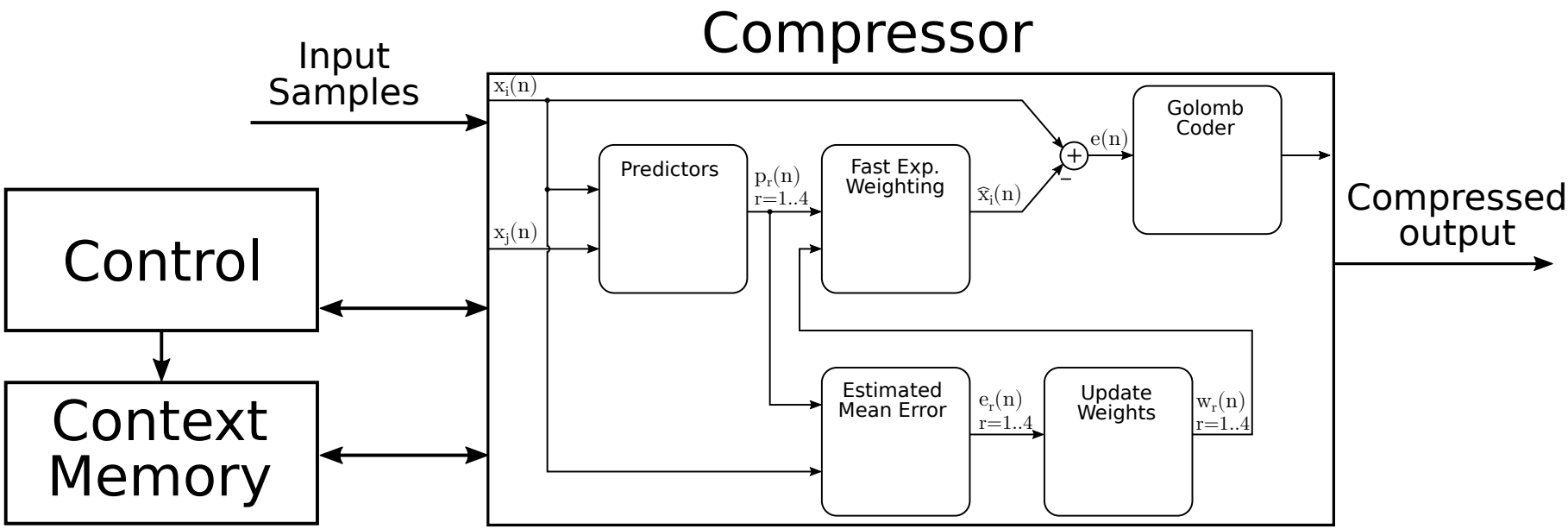


Low power architecture

- Sequential architecture: Need of saving compressor context.
- Reduced area to use a smaller chip: Lower power consumption, less cost.
- Set maximum sampling Rate: Use a Duty cycle (Sleep mode).
  - Sequential arq. for 21 ch. Max SR of 90 ksps.



Conclusions

- Successful hardware implementation of the algorithm.
- Parallel approach as a proof of concept.
- Tested on a Cyclone V FPGA:
  - Good results in terms of compression ratio and compression time per sample.
  - High power consumption (as expected).
- New approach to reduce power: Reuse resources (work in progress)
- Further analyze low power design on FPGA.
  - Comparison vs microcontrollers.

Thank you!
Questions?