AN APPLICATION OF THE HARDENED FLOATING-POINT CORES ON HIL SIMULATIONS

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Power converter

- Design
- Verification
  - Thousands of directed and random tests are typically required to test performance under normal and abnormal operating conditions.
HIL emulation

• For HIL applications, the controller is connected to a virtual plant executed on a real-time simulator, instead of to a physical plant.

Our goal...

• Is to develop a HIL converter model.
  • That is a verification device
  • AKA Verification IP

• … an accurate model for HIGH-speed applications!
Power electronic applications

- Accurately simulating fast-switching power electronic devices requires the use of very small time-steps to solve system equations.

Fast-switching power electronic apps.

- For example, the switching frequency is 40 MHz in

- And 75 MHz in
Simulation step

- At least 100 points per switching period are needed to obtain accurate enough results.
  - For example, a switching frequency is 100 kHz, requires an integration frequency of at least 10 MHz.
- So… simulation time-step can be very short
  - An integration frequency of 10 MHz means an integration step of 100 ns.

FPGAs came up to help

- FPGAs have many advantages for real-time simulation and are successfully applied on HIL systems since 2010.
But if floating-point is used…

- But even using FPGAs, it has not been possible to reach real time simulations when small integration steps are necessary (around 100 ns or lower) if floating-point representation is used.
Hardened floating-point

✓ Area + Performance + Design time

Study case

• Topology of a full-bridge converter
  • An algorithm defines d and q based on S1 to S4
  • The model needs to calculate the output voltage (Vout) and inductor current (iL) every time step, taking into account four configurations.
Study case: converter equations

- Output voltage for each time step $k$, regardless of the configuration:

$$v_{out}(k) = v_{out}(k-1) + \frac{\Delta t}{C} \cdot (i_L(k-1) - i_R(k-1))$$

- Inductor current when $dq = 10$, $dq = 01$, and $dq = 11$ or $dq = 00$, respectively:

$$i_L(k) = i_L(k-1) + \frac{\Delta t}{L} \cdot (v_g(k-1) - v_{out}(k-1))$$

$$i_L(k) = i_L(k-1) + \frac{\Delta t}{L} \cdot (-v_g(k-1) - v_{out}(k-1))$$

$$i_L(k) = i_L(k-1) + \frac{\Delta t}{L} \cdot (-v_{out}(k-1))$$

Study case: implementation

- Digital circuit
- Four HFPs...
Study case: verification

- The evaluation is done by collecting the state variable values, and comparing those values with those of a reference model.
- The reference model in VHDL is based on variables of real type and an integration step of 1.25 ns.
- Multiple simulations have been performed: input voltage transients, changes on the duty-cycle, load transients and also simulation of steady states.

Study case: results
Conclusions

• We have focused on a verification artifact: HIL converter models.
• Industry needs high-speed and accurate HIL models.
• Hardened floating-point cores are as fast as fixed-point implementations with a better design time…
• … but these HFP cores support single-precision IEEE 745 operations, with known accuracy issues.
• The problem of using wider variables is that, if a non-standard floating-point format were used, the model would not take benefit of the HFP cores, unless a sort of hybrid technique might be developed in the future.