Design for Portability of Reconfigurable Instrumentation Based on Programmable Systems-on-Chip

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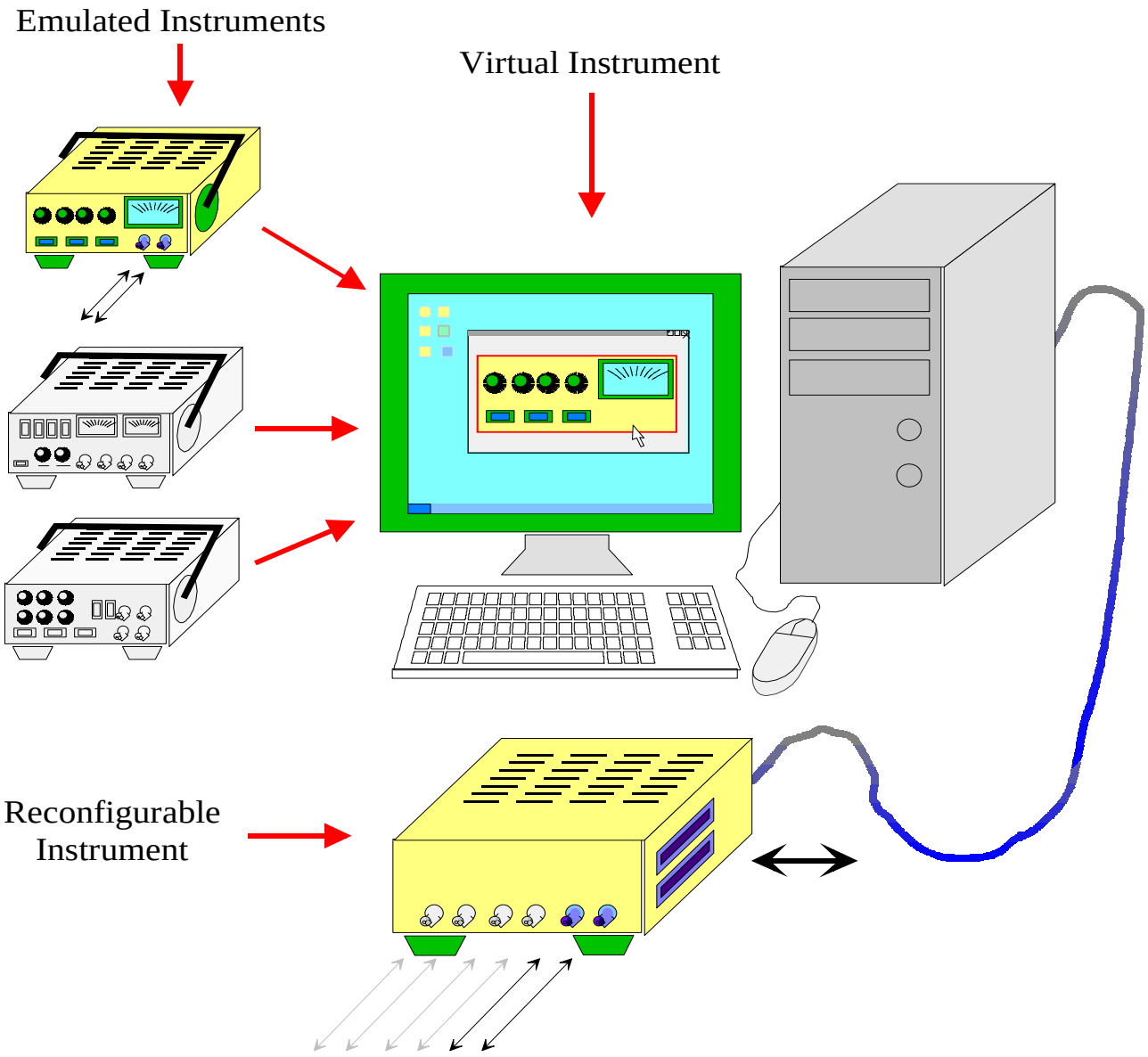
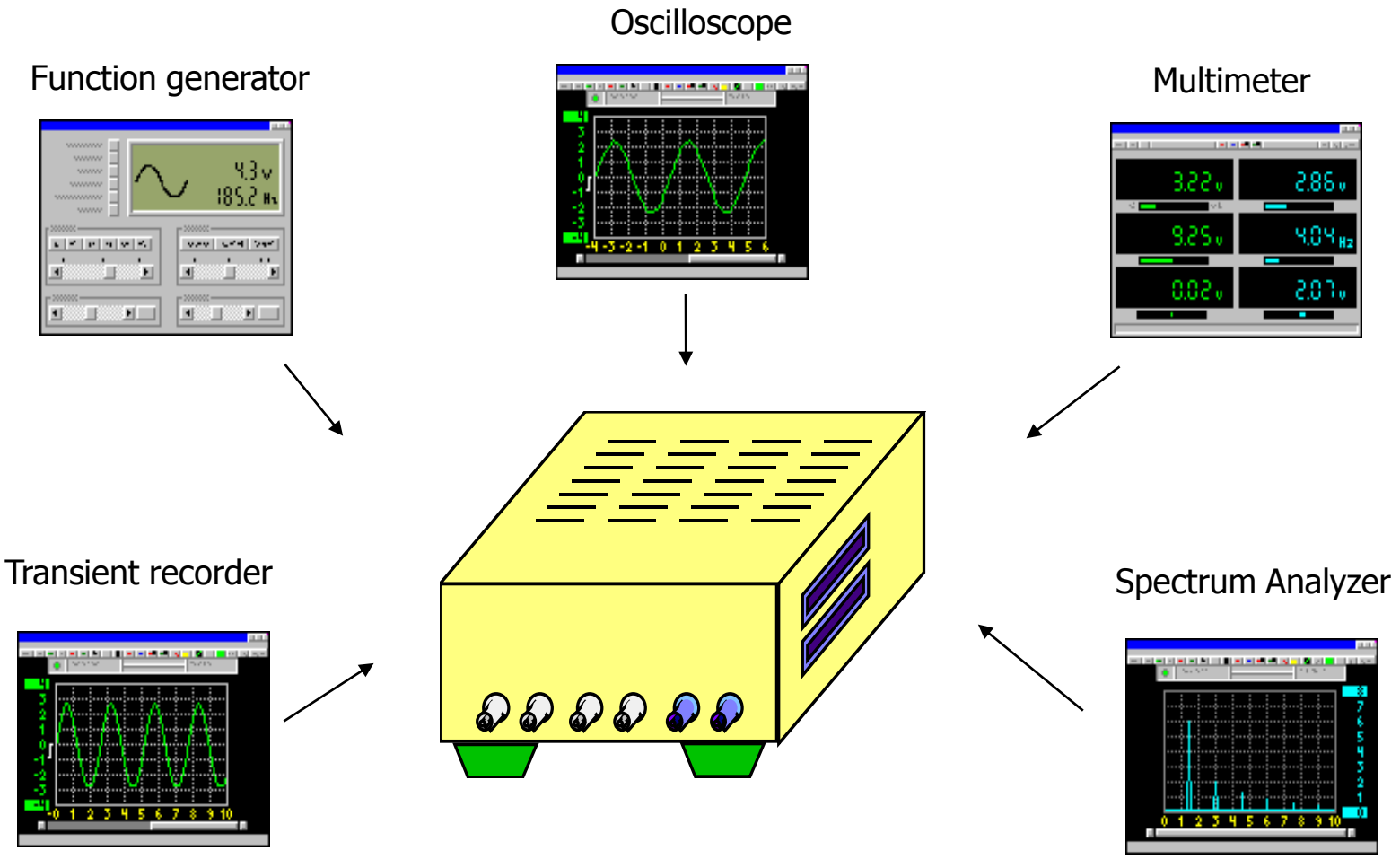
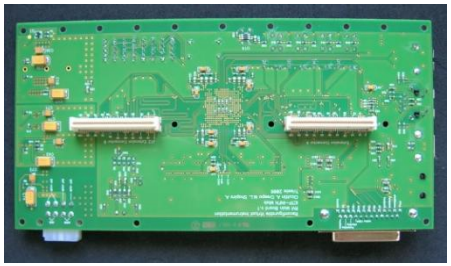
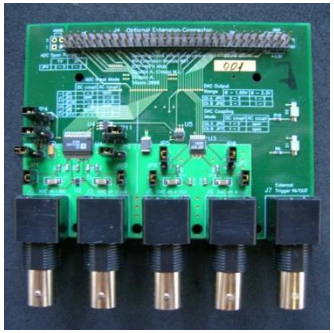
Reconfigurable Virtual Instrumentation

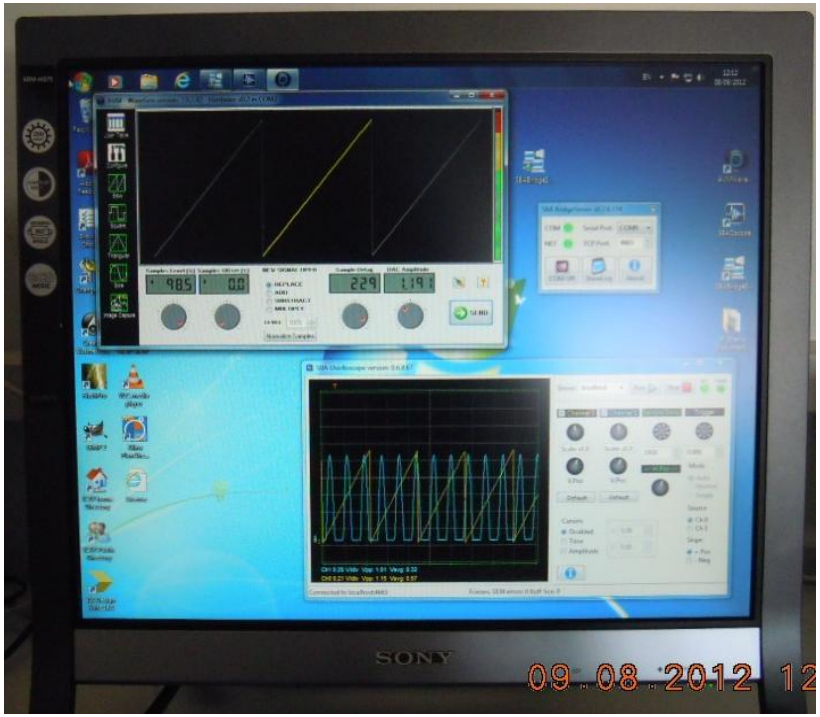


Reconfigurable Virtual Instrumentation



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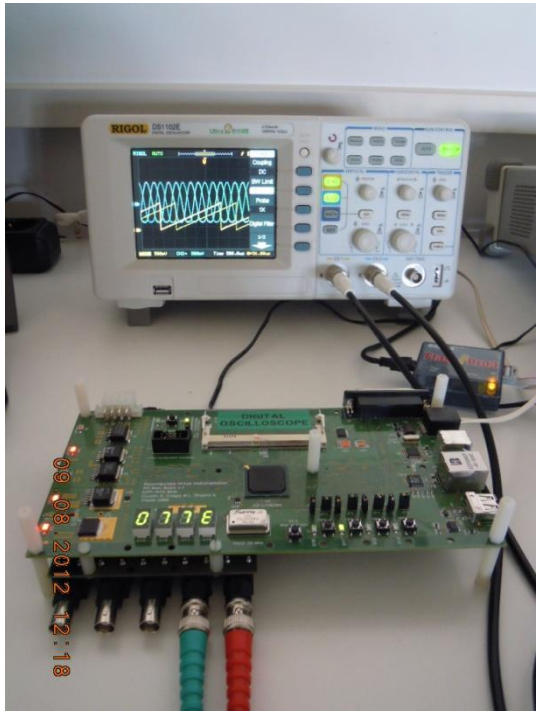
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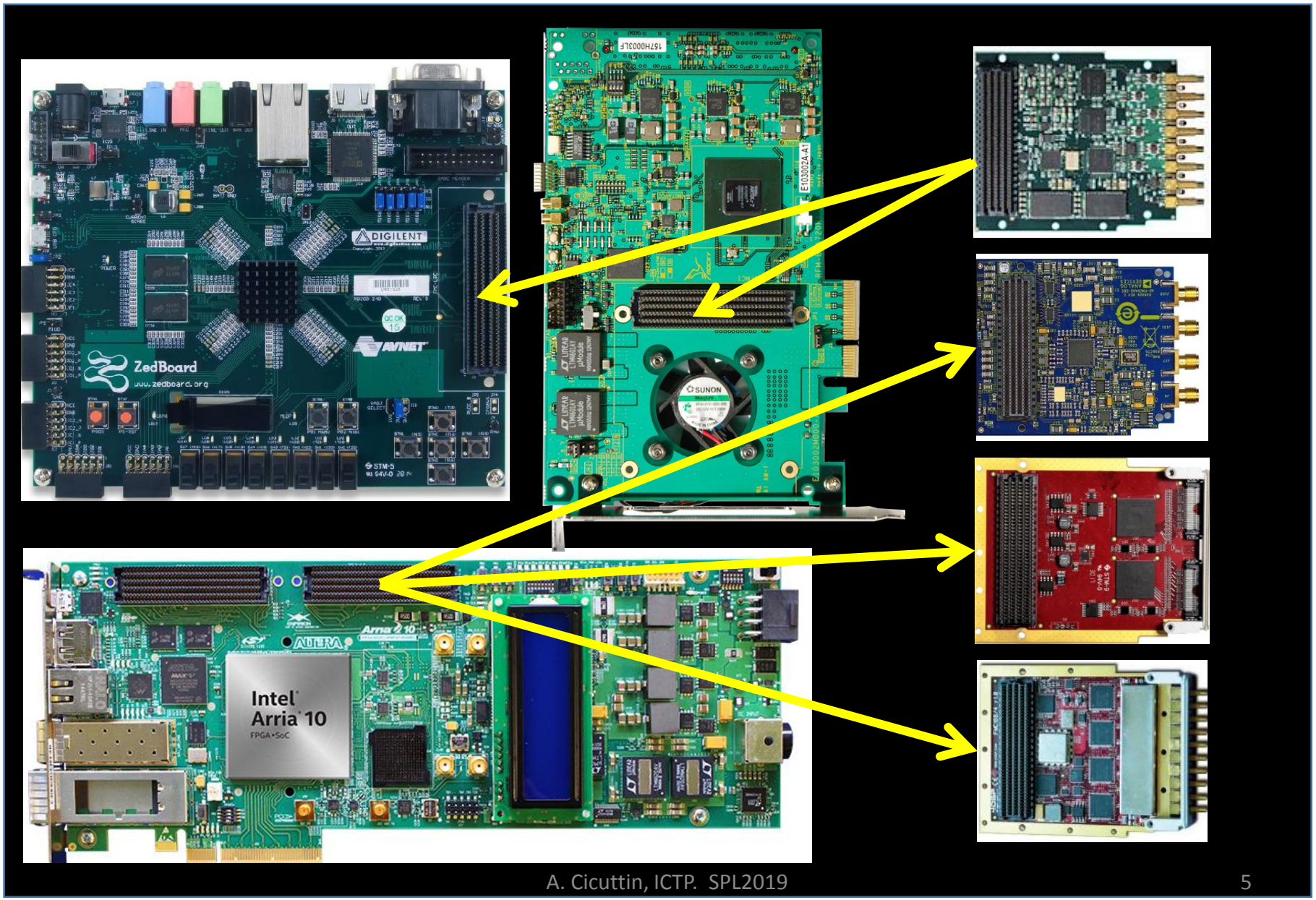
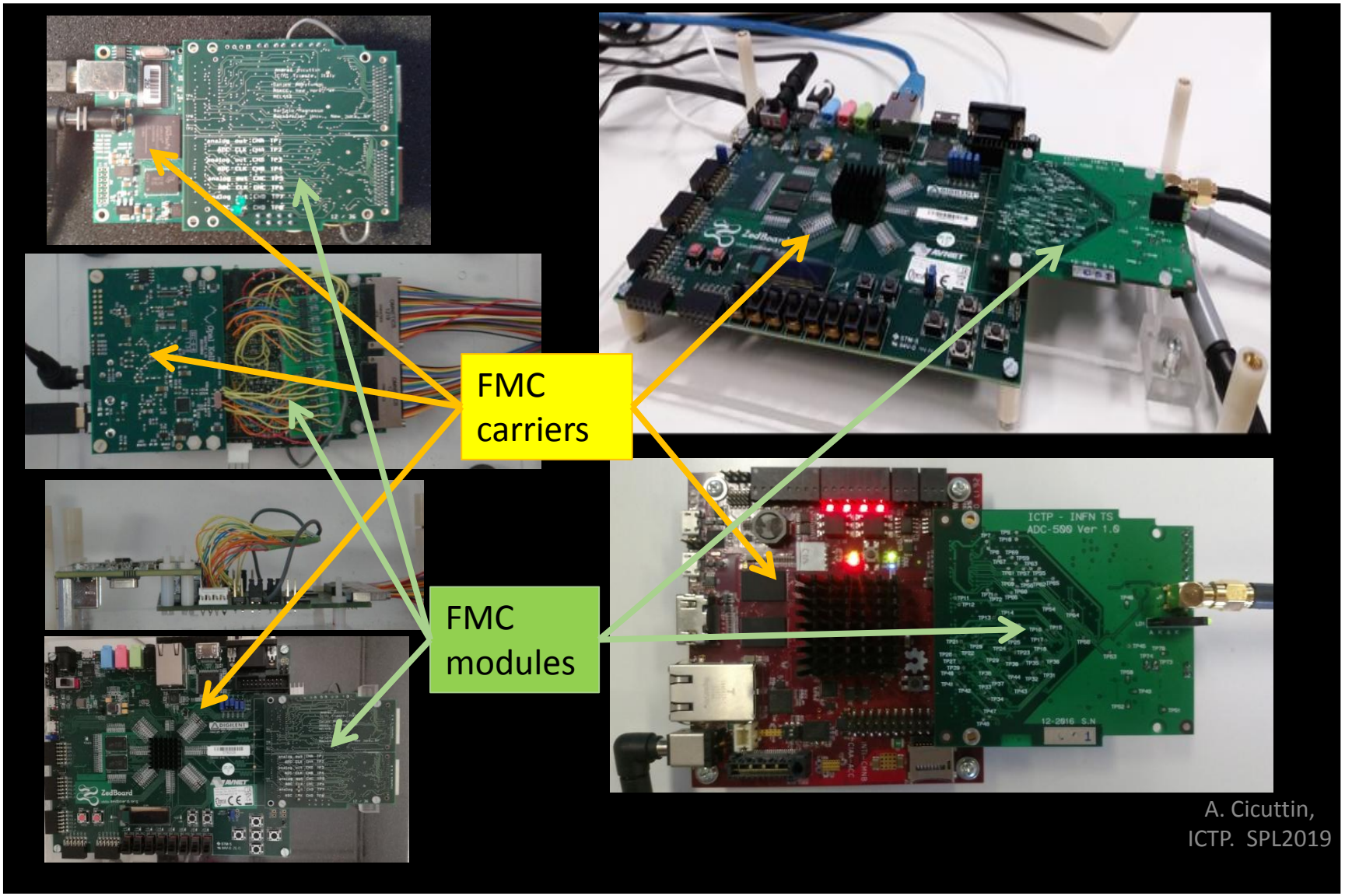
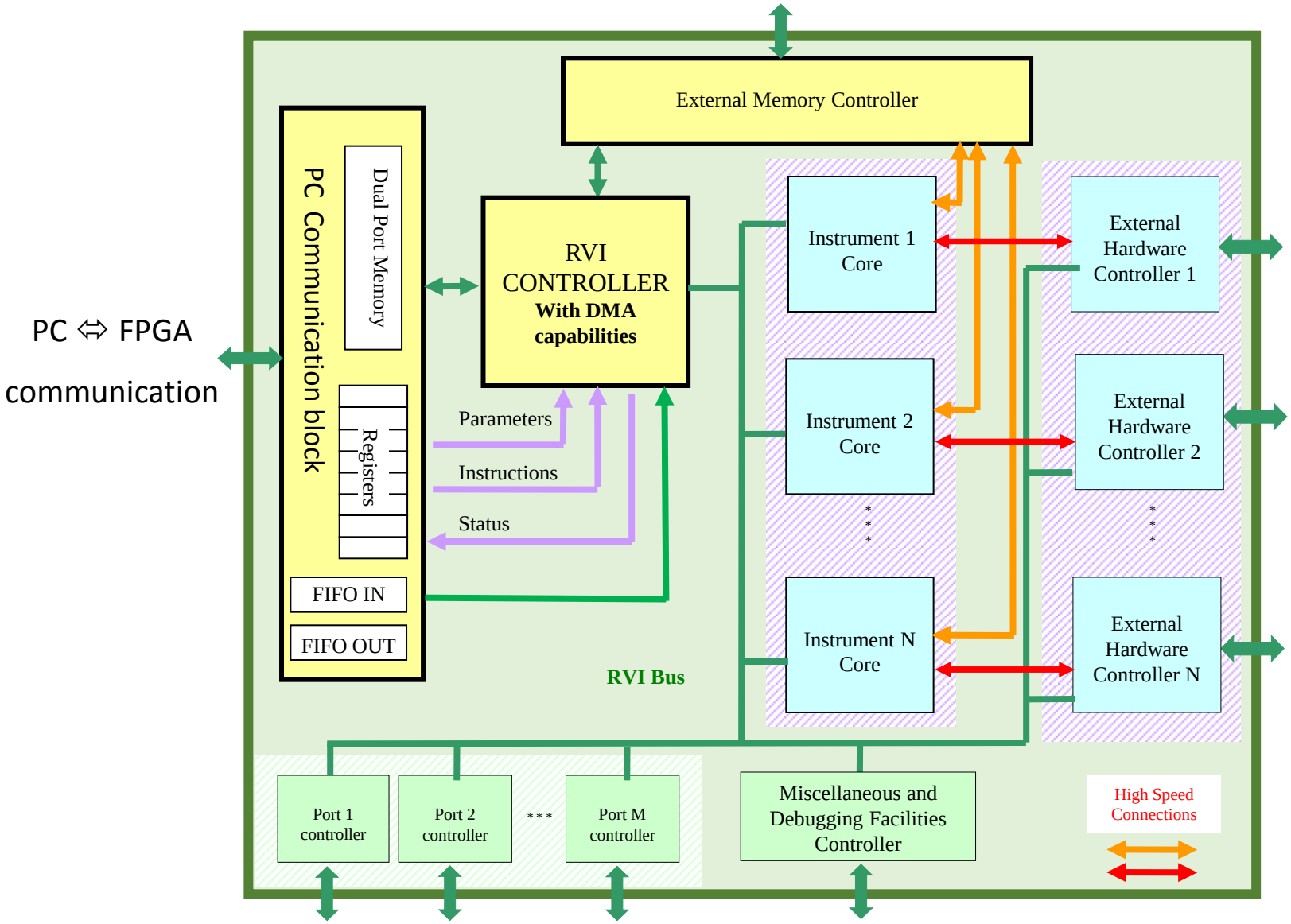
Hardware modularity and porting across different platforms



Portability among different FMC Carriers of instrumentation based on dedicated hardware modules



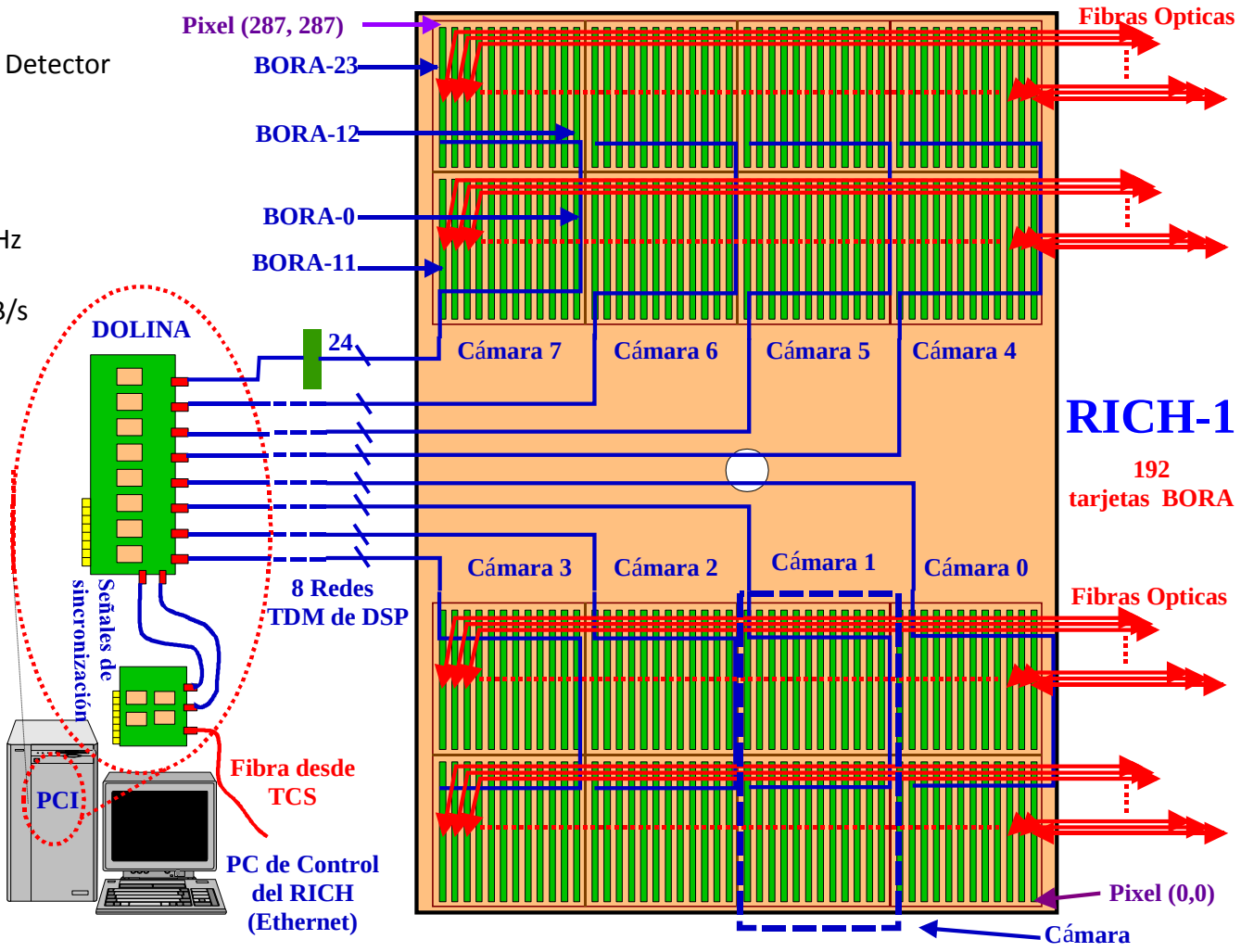
A possible FPGA Global Architecture for RVI



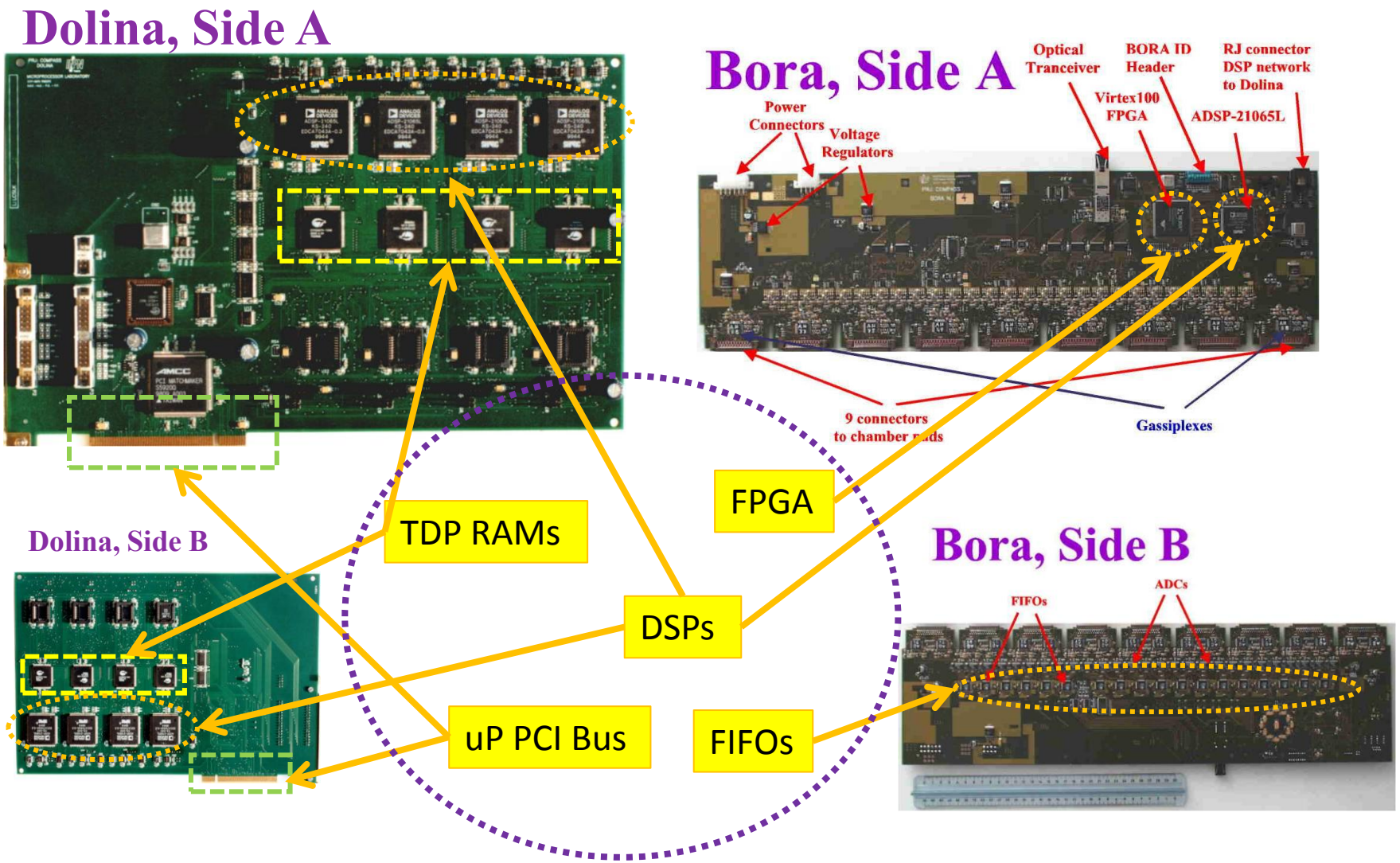
Global Architecture of a distributed instrumentation

DAQ System
Ring Imaging Cherenkov Detector
COMPASS Experiment
CERN, 2004.

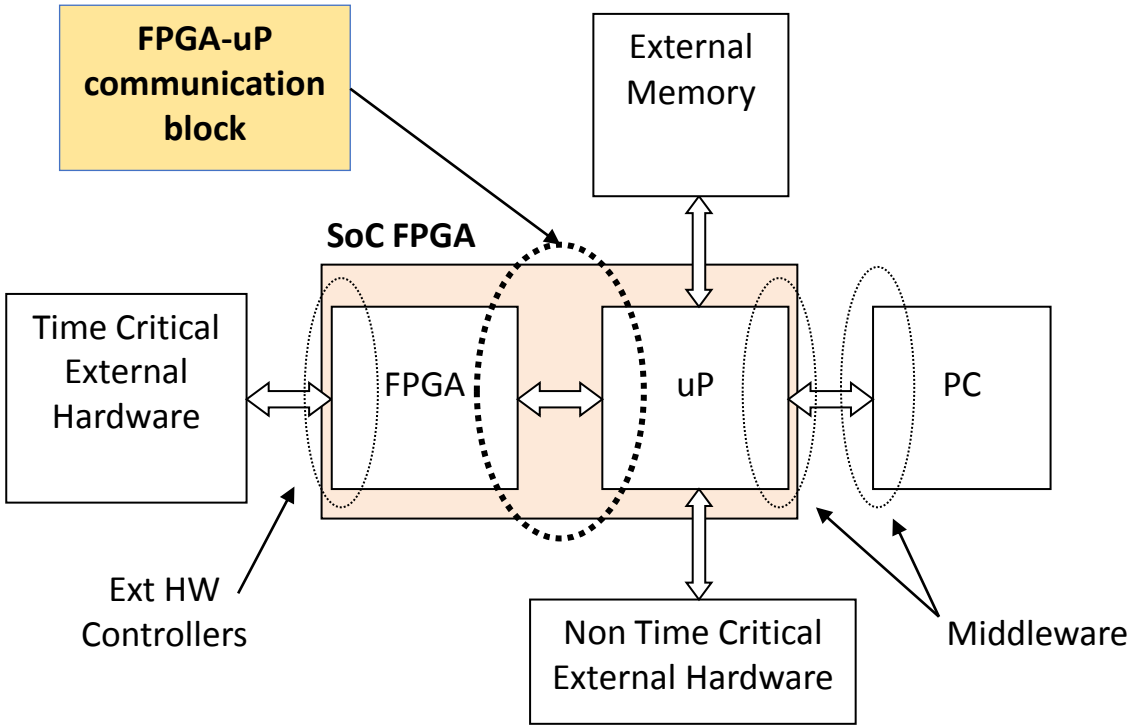
Pixels : ~ 80000
Ave trigger rate: ~ 100KHz
Dead time: ~ 1 us
Max data rate: ~ 100GB/s



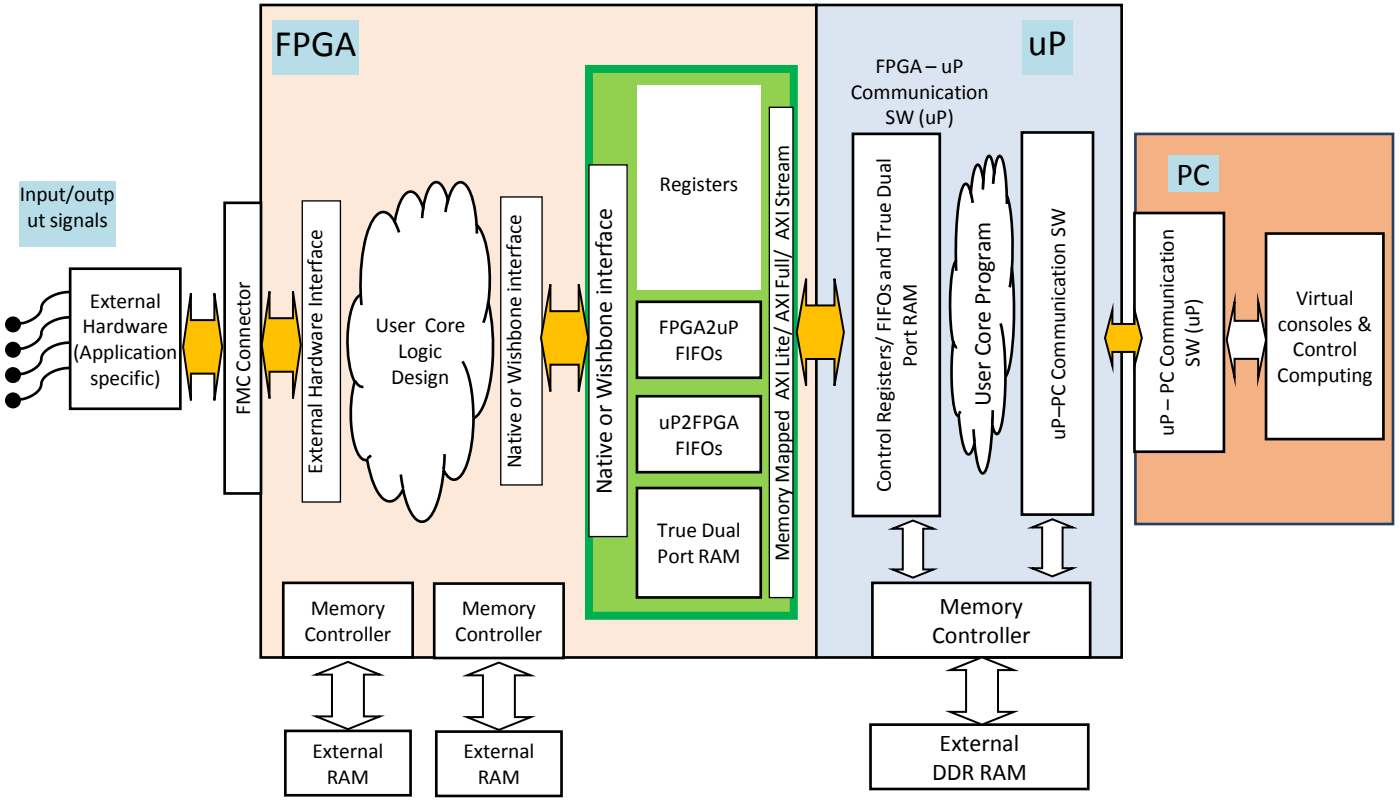
Data movement through distributed instrumentation



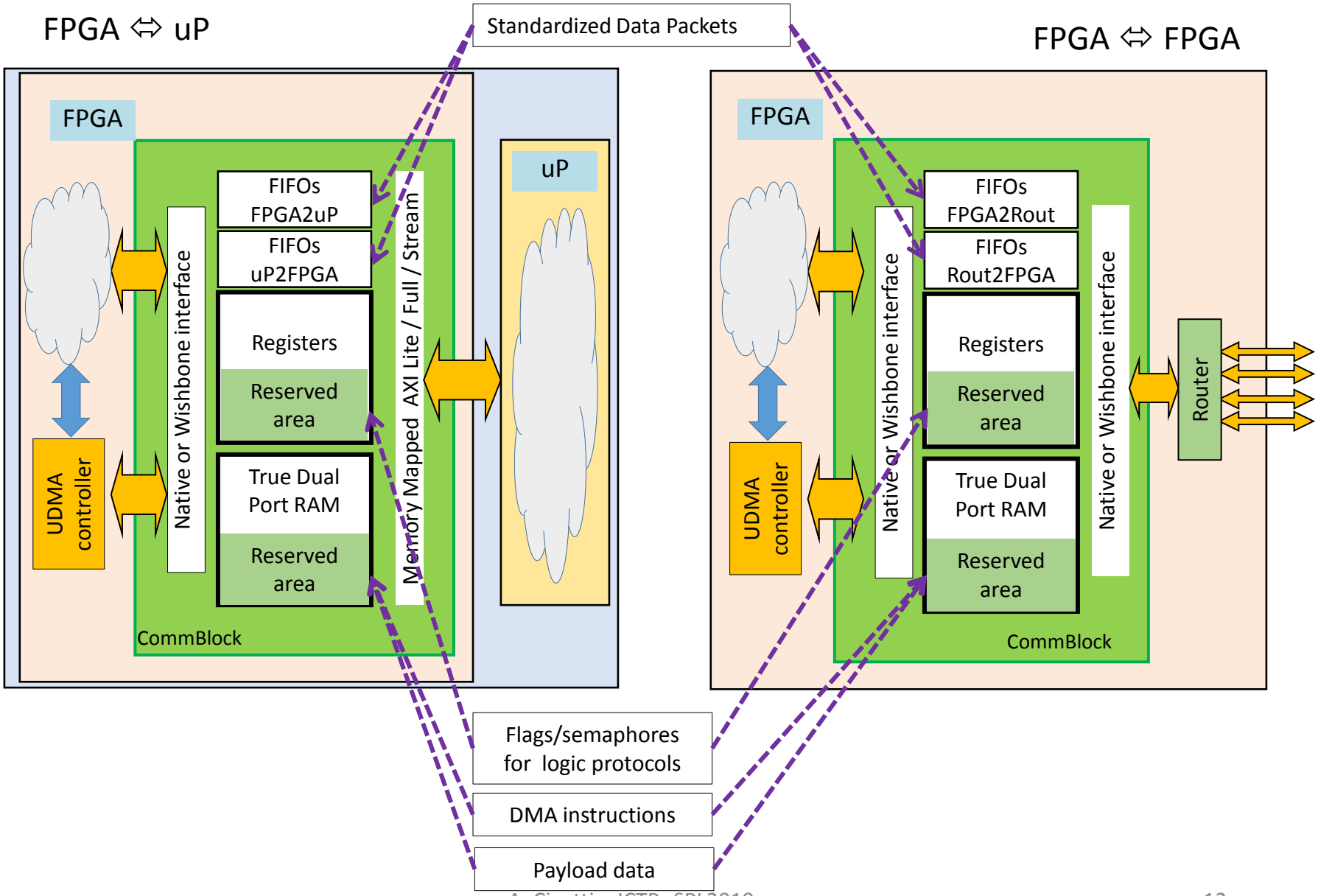
Reconfigurable Instrumentation based on SoC FPGA Global Architecture



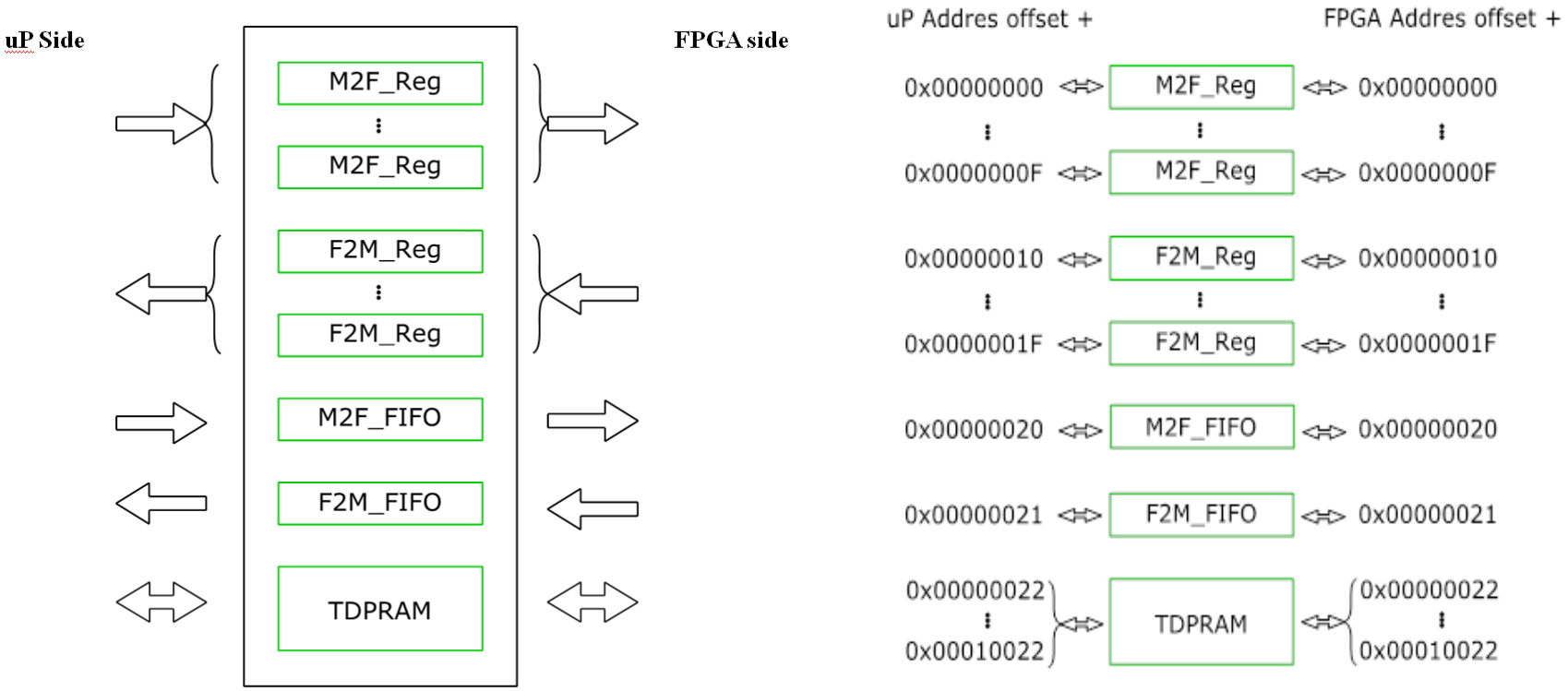
Reconfigurable Virtual Instrumentation Based on a single SoC FPGA Typical Global Architecture



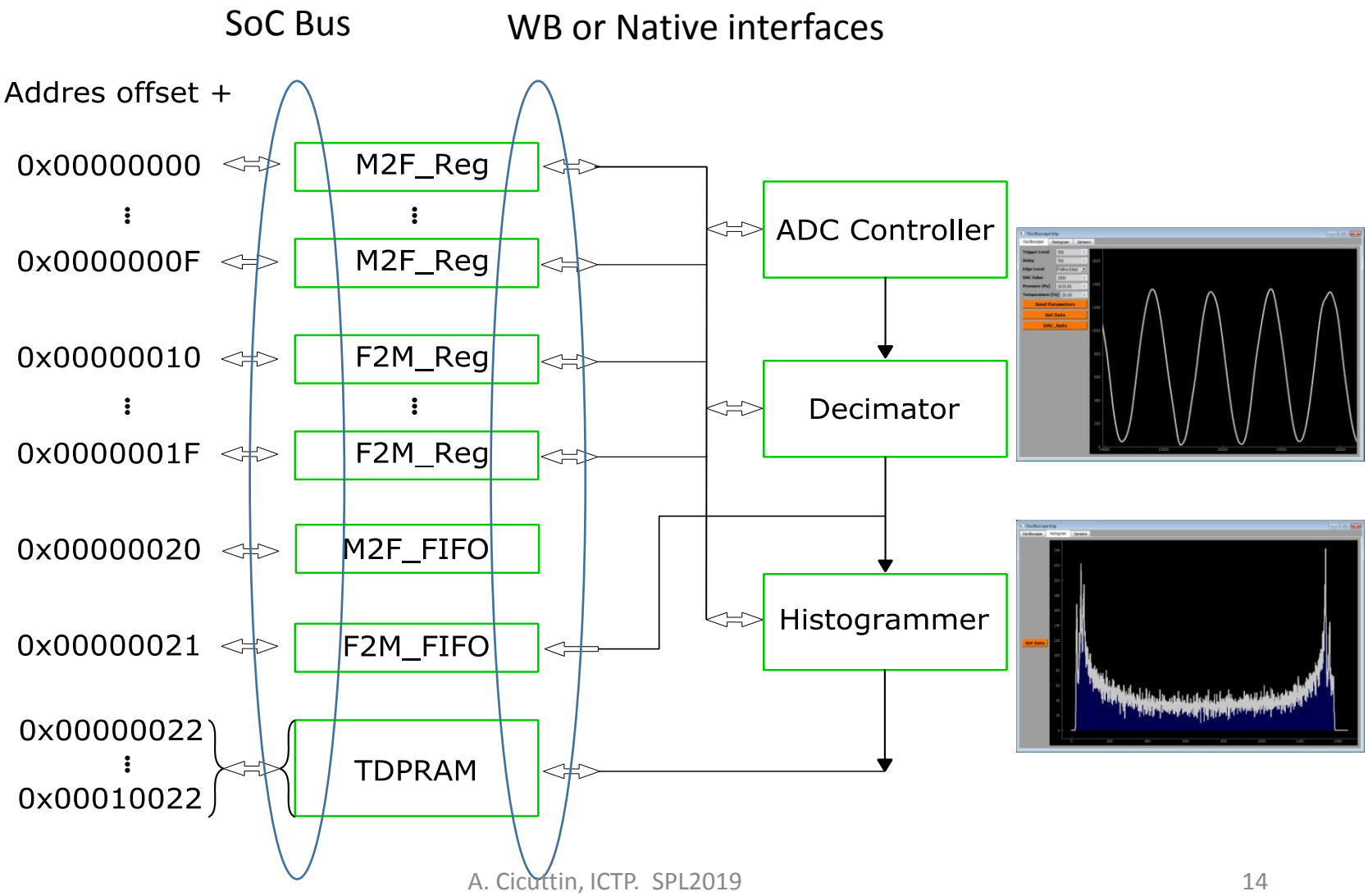
Reconfigurable Distributed Instrumentation Based on multiple SoC FPGA



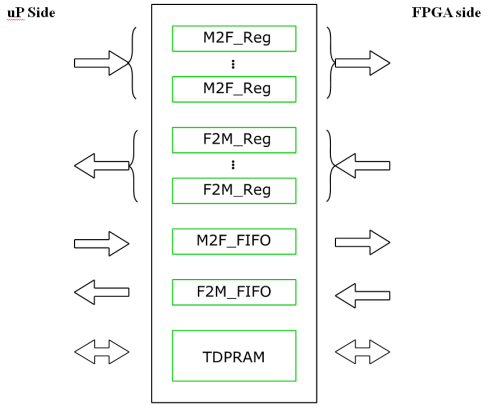
A block view of the **C**ommunication **B**lock and memory mapping of the **CB** ports

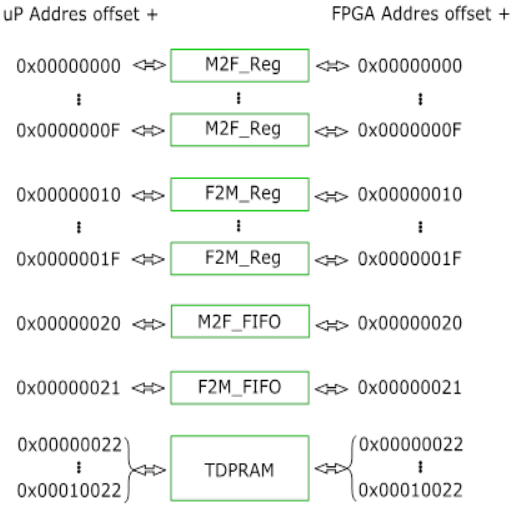


ComBlock: Memory mapping on the uP side, and its connections with functional blocks implemented in the FPGA.

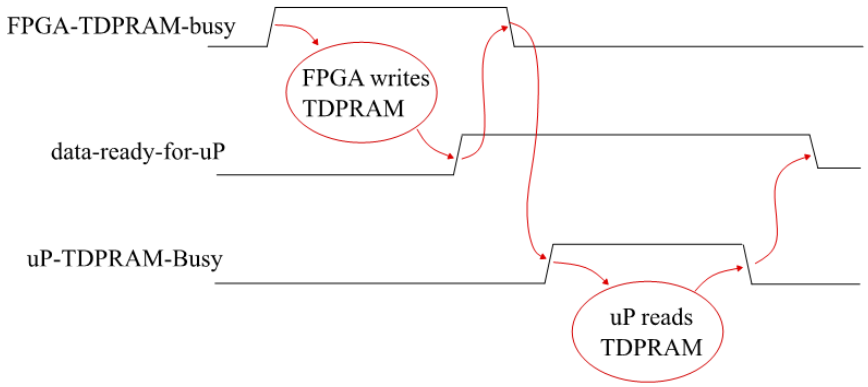


A possible logical utilization of reserved registers for safe data transfer through TDP RAM

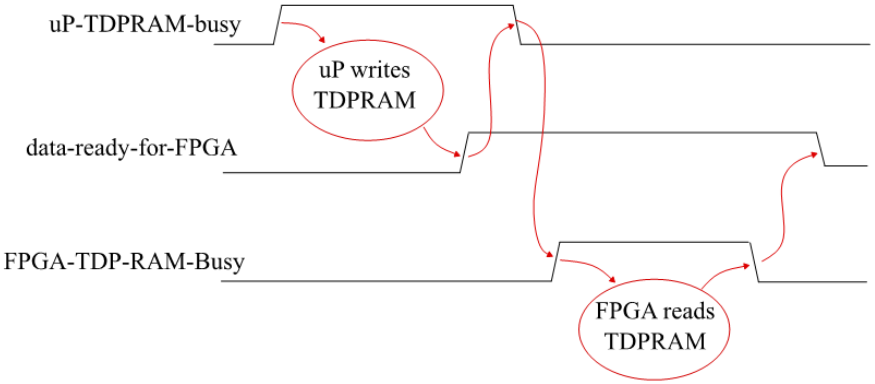




Data from FPGA to uP

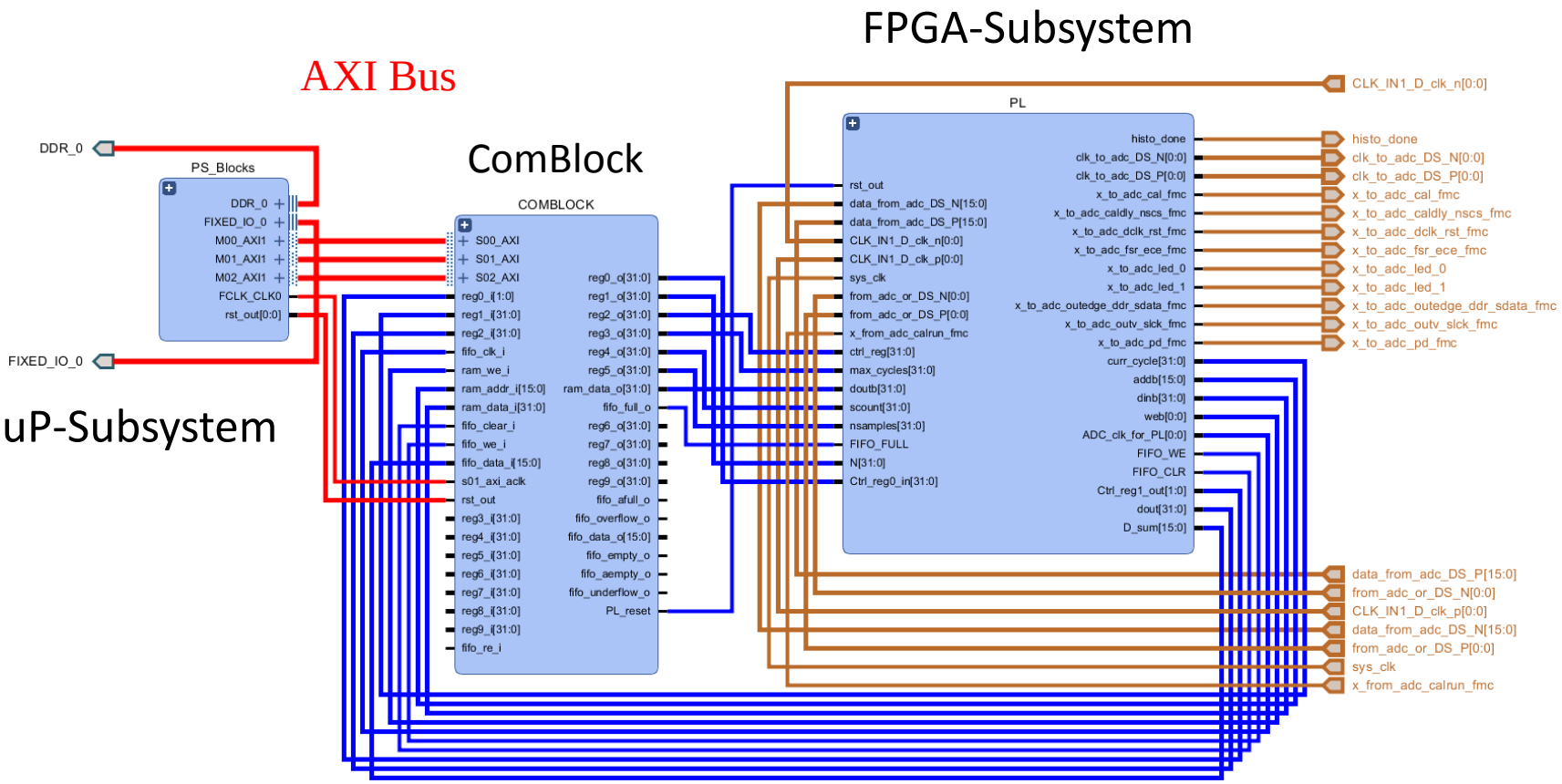


Data from uP to FPGA



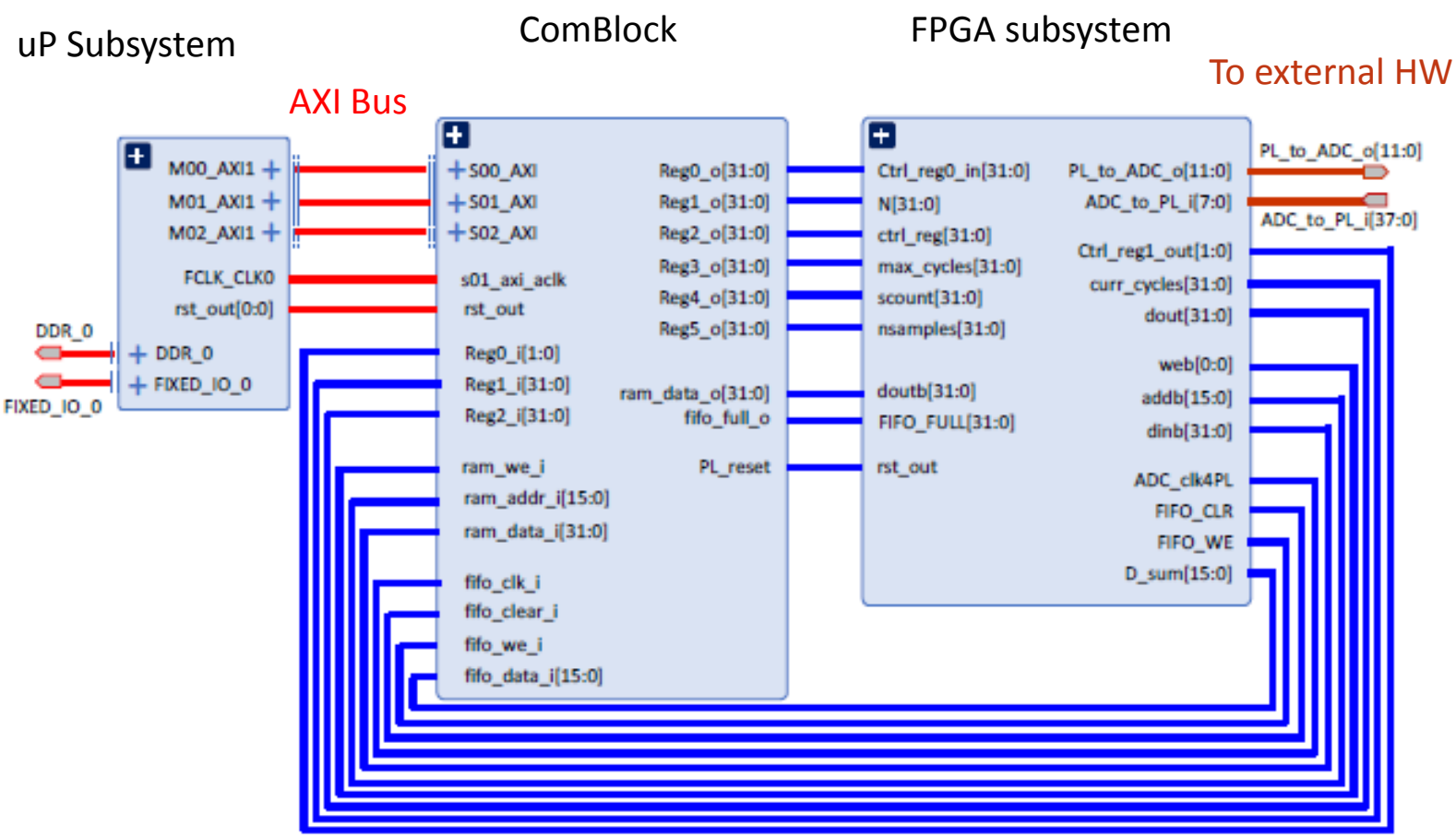
Asynchronous timing diagram of a flags-based protocol for safe data transmission through the TDPRAM of the CB

Top level schematic: ComBlock and its connections



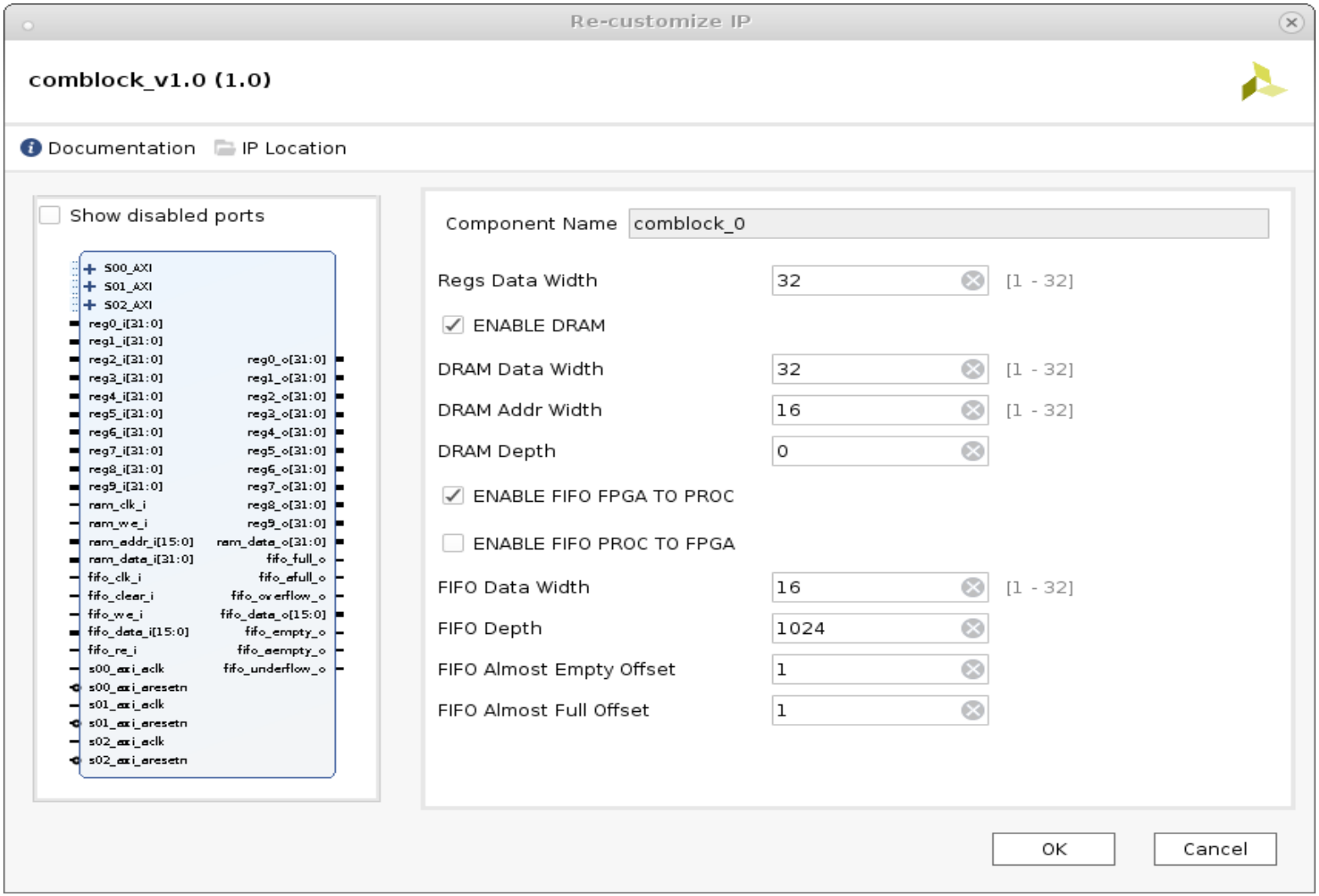
Custom connections with the FPGA-subsystem

Top level schematic: ComBlock and its connections



Custom connections with the FPGA-subsystem

Configuration wizard window for the ComBlock



(Vivado System Edition)

Communication between the FPGA and uP subsystems

It can be implemented by mean of three different hierarchical levels:

1. **Physical**

   Allows a simple utilization of the resources of the CB as storage elements.

2. **Logical**

   Includes a basic asynchronous logic protocol for a safe utilization of the ComBlock. It requires some reserved areas in the TDPRAM and some reserved registers.

3. **Systemic**

   Implements a high level protocol based on a set of complex instructions for Direct Memory Access (DMA). It provides transparent access from any domain to all resources mapped in a global memory mapping, including those that are not immediately accessible but that are directly accessible from the other domain. It requires a DMA machine in the FPGA, and a corresponding software routine in the uP.

Each level corresponds to a communication layer. Each layer relays on the services offered by the immediate layer below, and provides services that can be used by the layer immediately above.

Resource utilization of the CB in different Devices

•RESOURCE UTILIZATION OF THE CB IN XILINXFPGAS

Family	Name	Slice LUTs	Slice Registers	F7 Muxes	F8 Muxes	Block RAM (kBytes)
Zynq-7000	xc7z020	726	816	128	64	290.25
Spartan-7	xc7s100	726	816	128	64	290.25
Artix-7	xc7a200	726	816	128	64	290.25
Kintex UltraScale+	xcku15p	854	816	128	64	290.25
Virtex UltraScale+	xcvu13p	854	816	128	64	290.25

•RESOURCE UTILIZATION OF THE CB IN ALTERA FPGAS

Family	Name	ALMs	Logic Registers	Block RAM (kBytes)
Cyclone V	5CSEMA5F31C6	764	563	290.25
Cyclone 10 LP	10CL006YU256A7G	1170	559	290.25
Cyclone IV GX	EP4CGX15BF14A7	1171	559	290.25
Cyclone IV E	EP4CE6E22A7	1170	559	290.25

Resource usage of a high-speed data acquisition system without and with the communication block

Name	Without Communication Block				With Communication Block			
	FPGA_ Subsystem	uP_ Subsystem	Others	Total	FPGA_ Subsystem	uP_ Subsystem	Communication _Block	Total
Slice LUTs	187	960	6691	**7838 (14.73%)**	186	1466	834	**2486 (4.67%)**
Slice Registers	264	1244	12696	**14204 (13.35%)**	264	1957	884	**3105 (2.92%)**
F7 Muxes	0	62	0	62 (0.23%)	0	62	128	190 (0.71%)
F8 Muxes	0	0	0	0 (0%)	0	0	64	64 (0.48%)
Block RAM Tile	0	0	66.5	66.5 (47.5%)	0	0	65	65 (46.43%)

Conclusions

1. The proposed *Communication Block is* a general purpose and reusable IP which completely absorbs the complexities of the *SoC Interconnection Bus* in modern SoC FPGA devices.
2. FPGA and uP subsystems can efficiently communicate through a *ComBlock* without any significant loss in performance and without any penalty in resources utilization.
3. Migration of complex systems among different SoC FPGA families and vendors is easier when based on *ComBlocks* since it essentially requires the porting of the *ComBlock* only.
4. Most of the uP embedded software and FPGA subsystem designs can be ported with minimal effort, and with facilitated debugging and optimization.
5. Since each subsystem deals with the other subsystem by reading and writing in the memory locations of the *ComBlock*, this block provides an abstract view of one subsystem to the other interacting subsystem.
6. The use of a ComBlock imposes a structured design methodology by mean of an explicit separation of the work in the uP and FPGA domains.
7. The implicit *ComBlock* strategy could simplify concrete Hardware/Software partitioning and implementation of complex cooperative activities.

Thank you for your attention!