

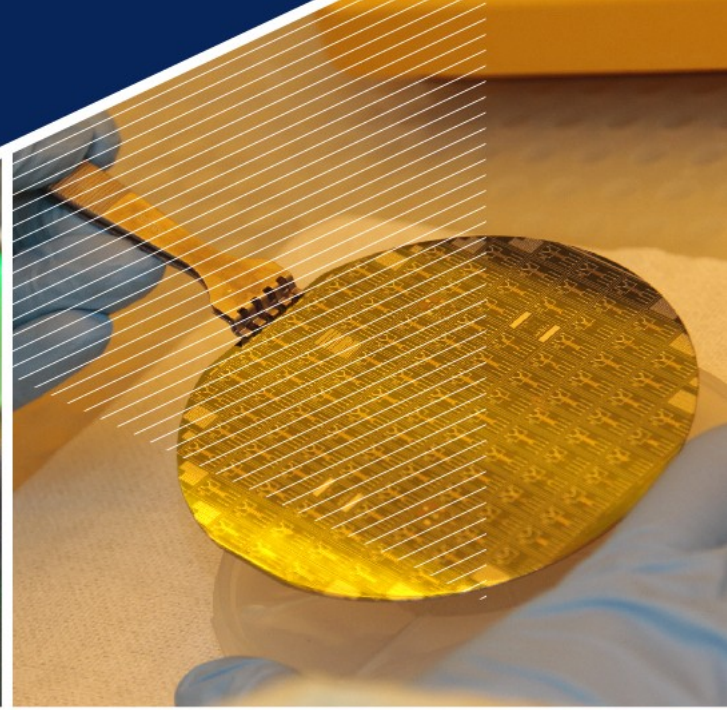


Serial QDR LVDS High-Speed ADCs on Xilinx Series 7 FPGAs

Bruno Valinoti, Rodrigo Melo

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Outline

Proposed system

- Requirements, High speed, SNR and resolution.
- Abaco (4DSP) approach & problems
- Proposal
- Virtex 6
- Zynq7000 series

Outline

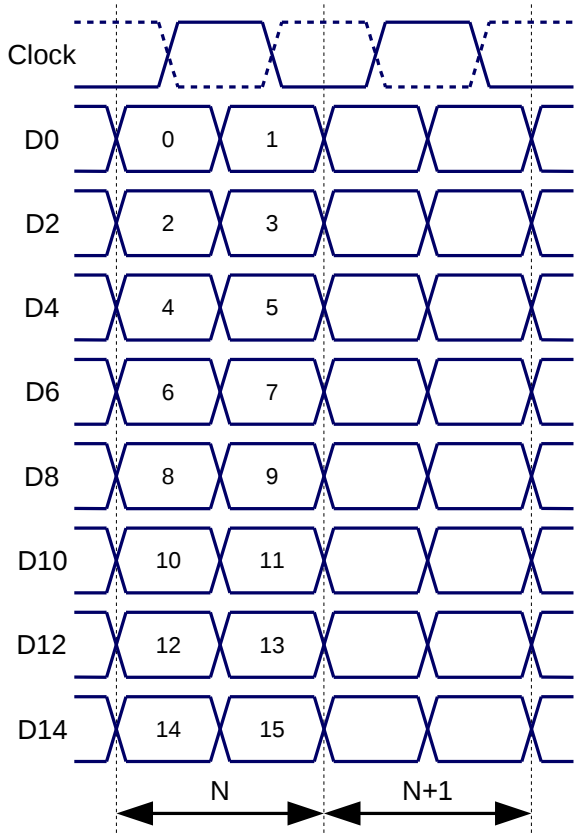
Board specification

FMC164 Analog Inputs	
Channels	4
Resolution	16 bits
Input voltage range	1Vp-p (4dBm) to 2Vp-p (10 dBm) programmable
Input gain	Programmable from -2dB to 6dB in 0.5dB steps
Input impedance	50Ω
Analog input bandwidth	500MHz (typical)
ADC Output	
Output data width	QDR LVDS mode; 4-pairs DDR per channel
	DDR LVDS mode; 8-pairs DDR per channel
Data Format	Offset binary or 2's complement
Sampling Frequency Range	250MHz internal clock
	Up to 250MHz external clock

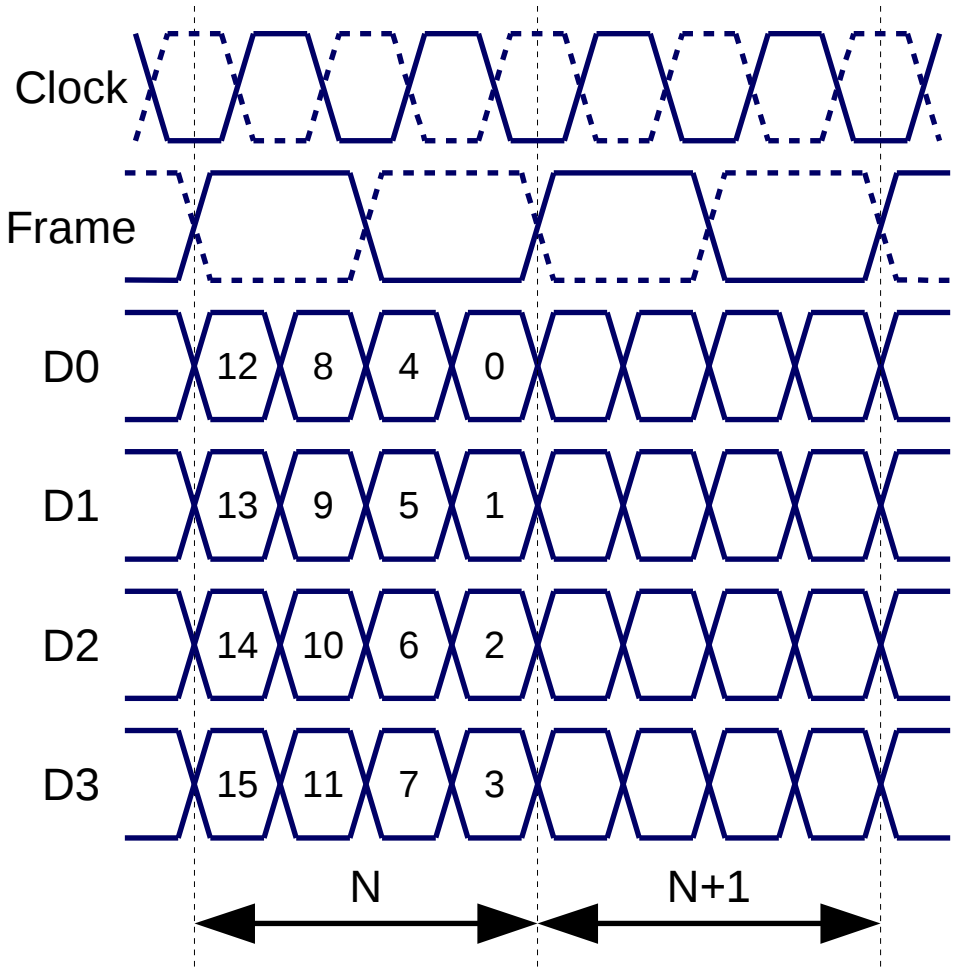
ADC specifications

ADS42LB69	
Channels	2
Resolution	16 bits
Input voltage range	2-V PP and 2.5-V PP Diff Full-Scale Input
Maximum clock rate	250 MSPS
SNR	72.3 dBFS @ 230MHz
Output Interface	DDR or QDR LVDS
Input impedance	1.2kΩ (differential)

Framing features I DDR



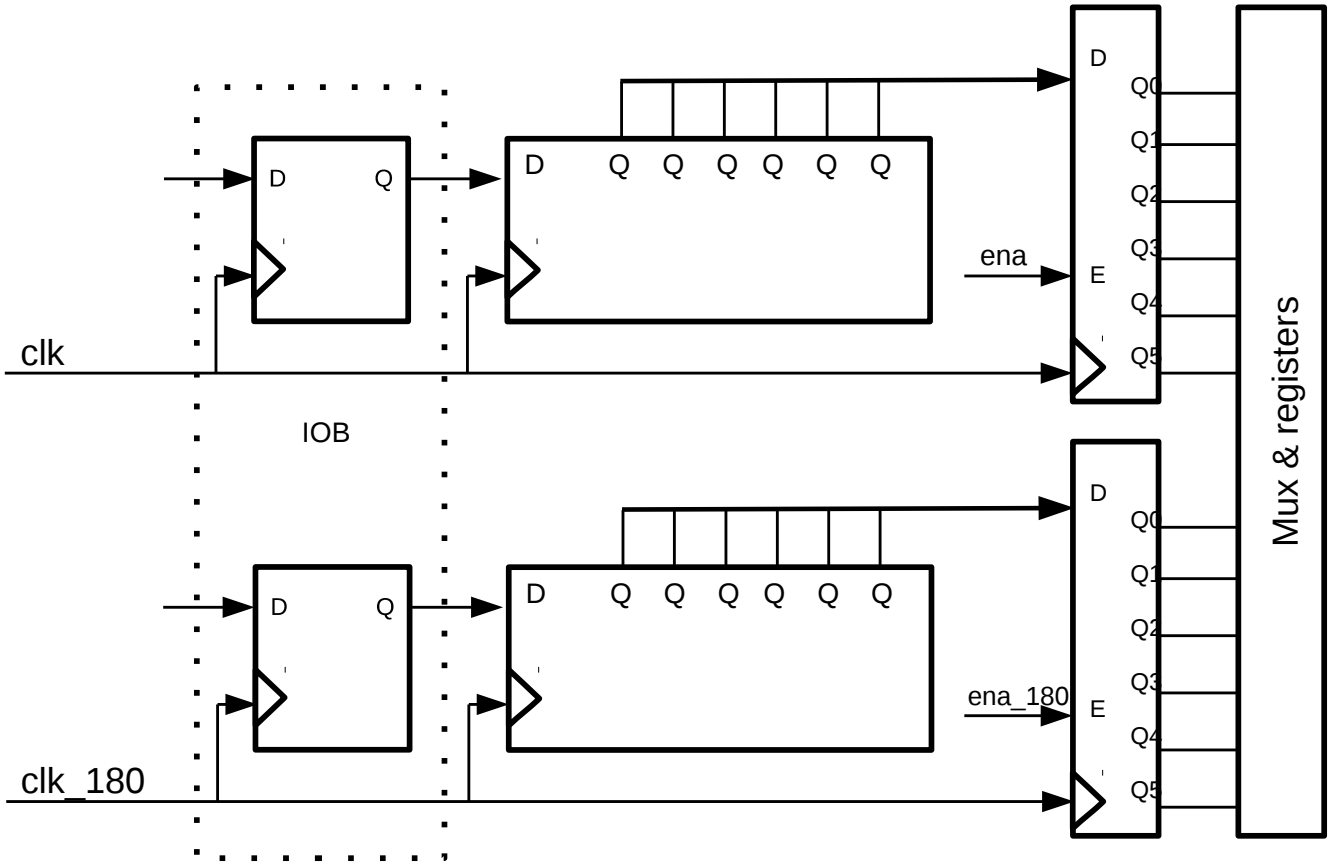
Framing features II QDR



Outline

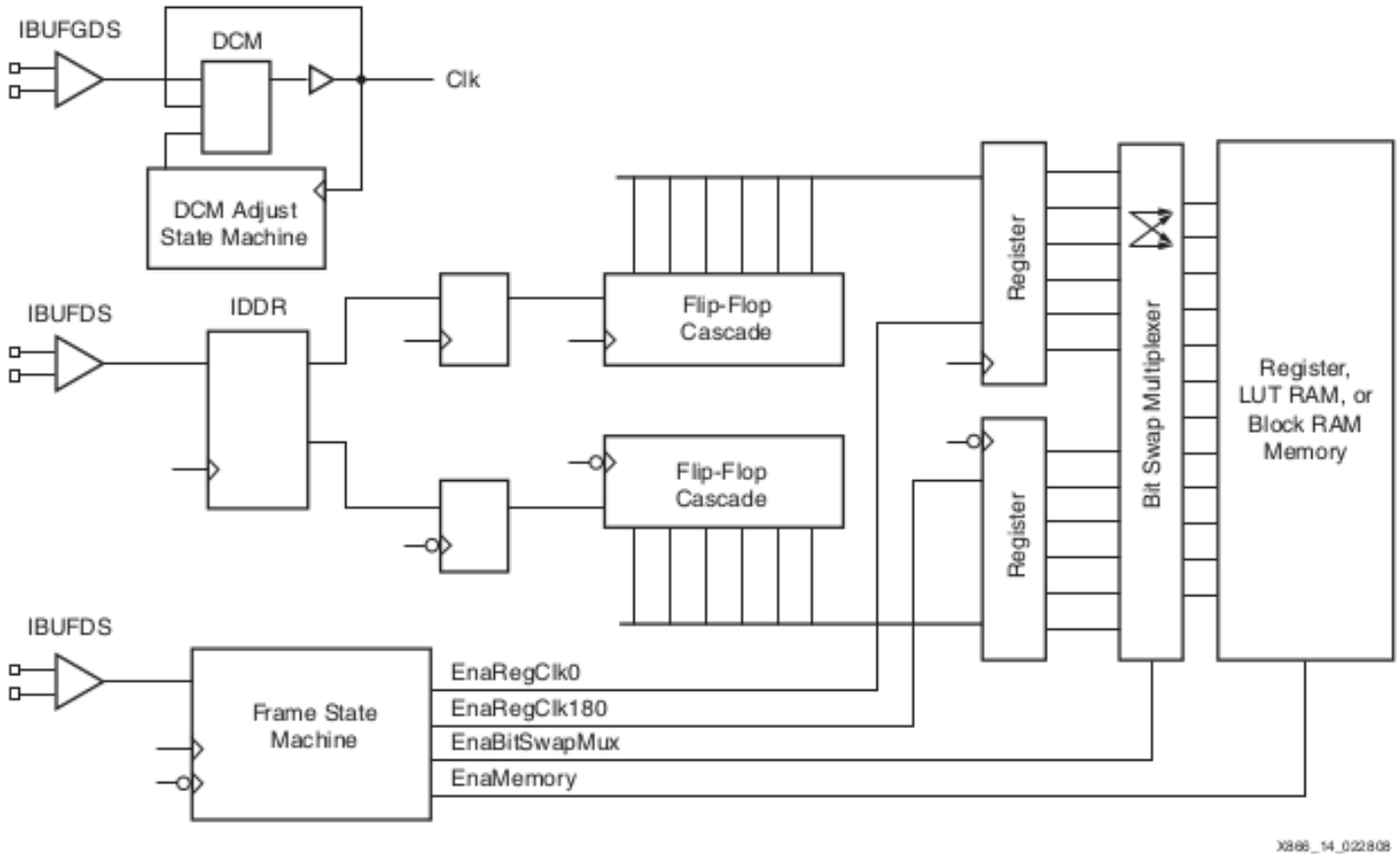
Virtex II and Spartan 3

Scheme used in the application note XAPP774.



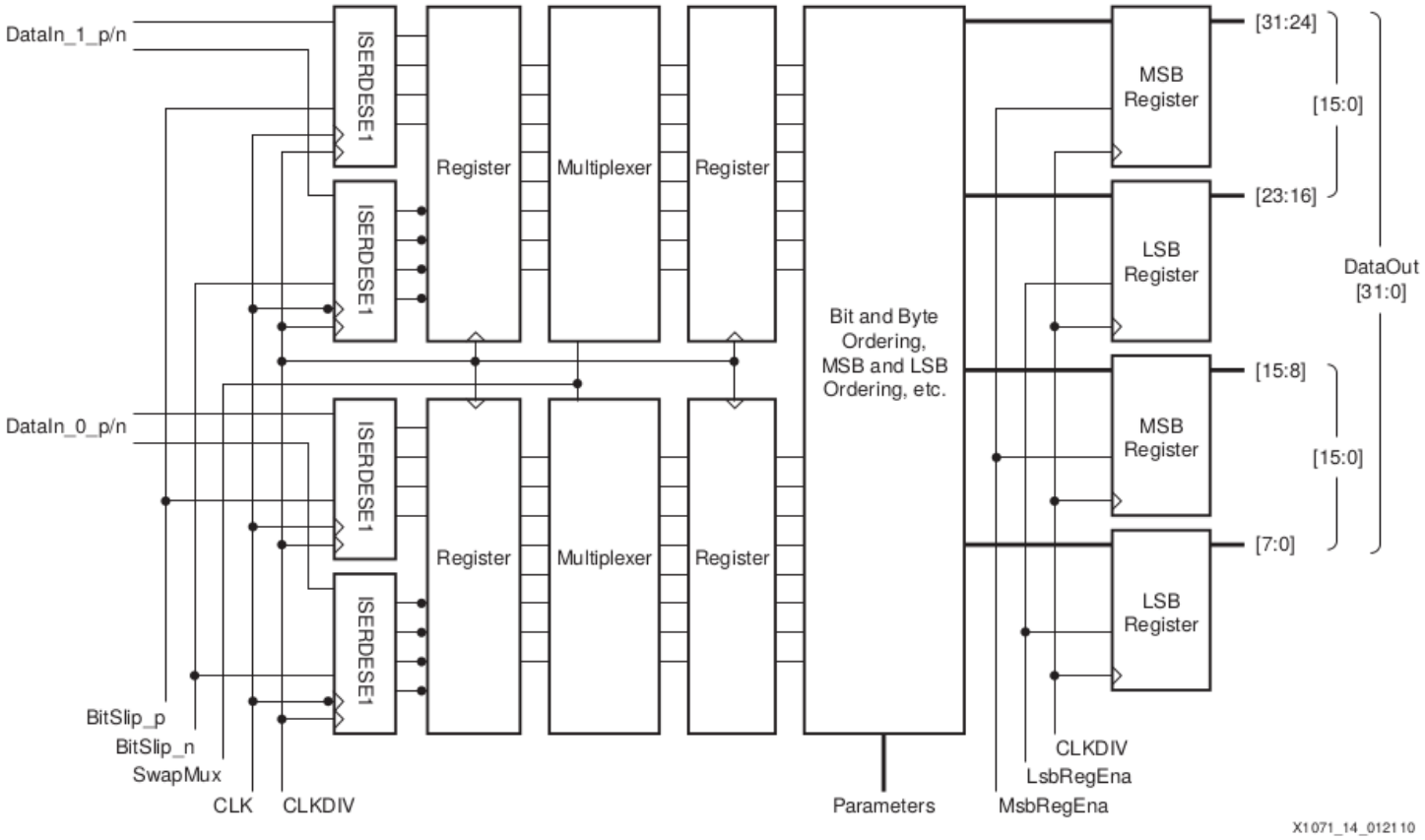
Virtex 4 and Virtex 5

Scheme used in the application note XAPP866.



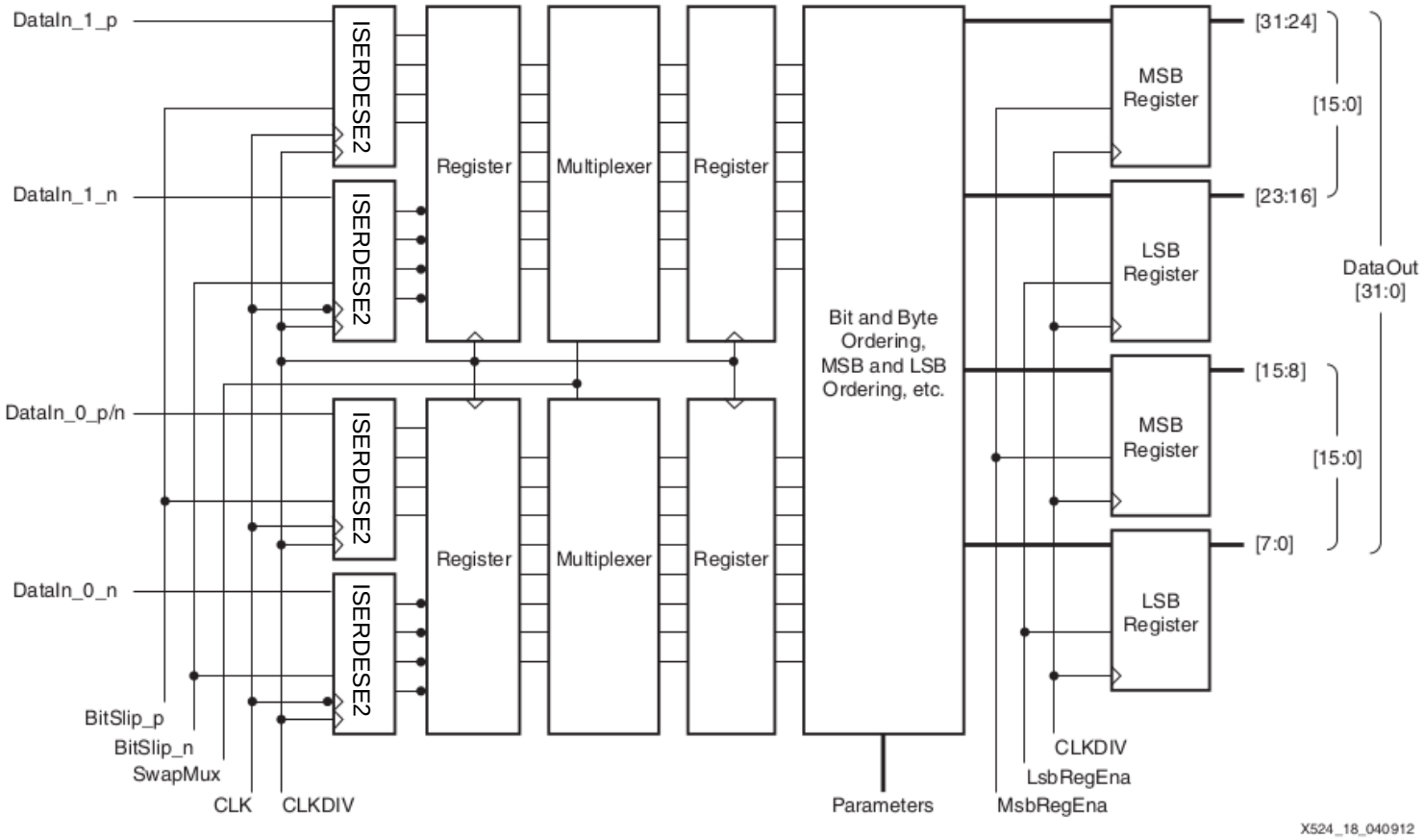
Virtex 6

The application note XAPP1071 shows a more sofisticated scheme:



Xilinx Series 7

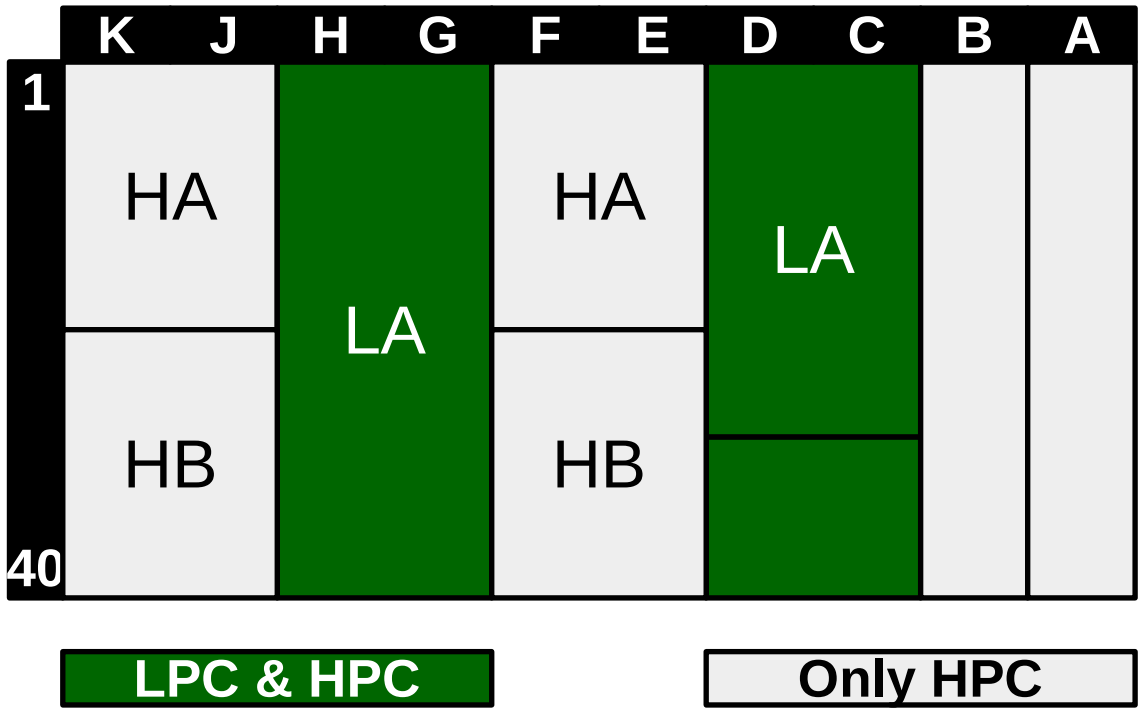
The application note XAPP542 shows a very similar scheme like the XAPP1071.



Outline

Hardware connectios

- FMC164
- ZC706
- FMC
- DDR vs QDR
- framing signals



To get 16-bit values with a sampling clock of 250 MHz, the clock provided by the ADC run at 500 MHz to read 4-bit as DDR two times, known as QDR mode.

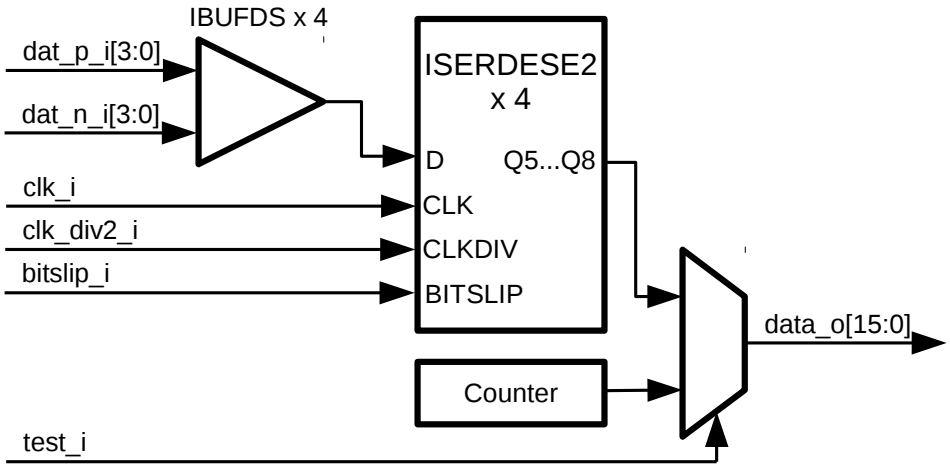
IP Modules (I)

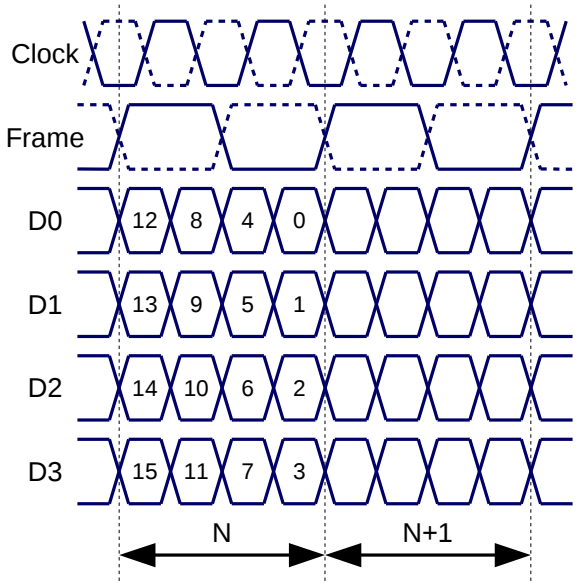
- adc_data.vhdl
- adc_frame.vhdl
- adc_cdc.vhdl
- adc_clock.vhdl

IP Modules (II)

- **IBUFDS:** differential input buffer.
- **IDELAYE2:** allows an input signal to be delayed.
- **IDELAYCTRL:** calibrates IDELAYE2, reducing effects of process, voltage, and temperature variations.
- **ISERDESE2:** a serial-to-parallel converter.
- **IN_FIFO:** very small FIFOs, designed for memory applications but available as general resource.
- **ODDR:** logic to implement an output DDR register.
- **BUFG:** global clock buffer.
- **BUFIO:** I/O clock buffer.
- **BUFR:** regional clock buffer.

Data deserializer



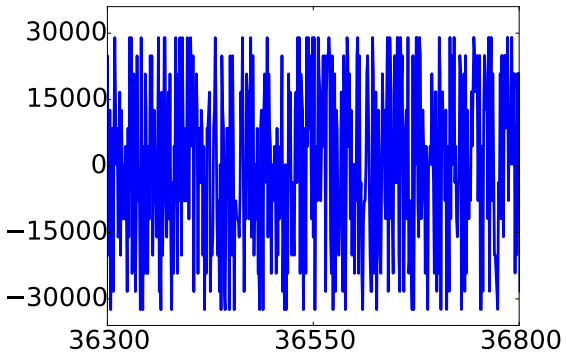


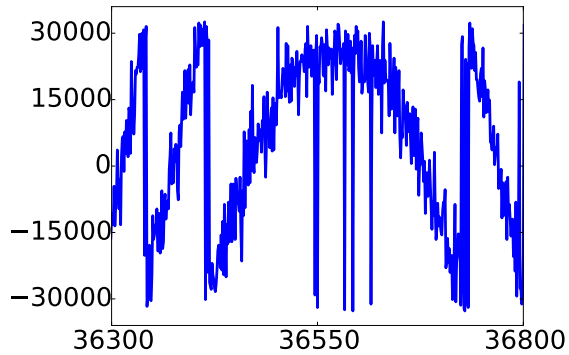
Syncronization and CDC (I)

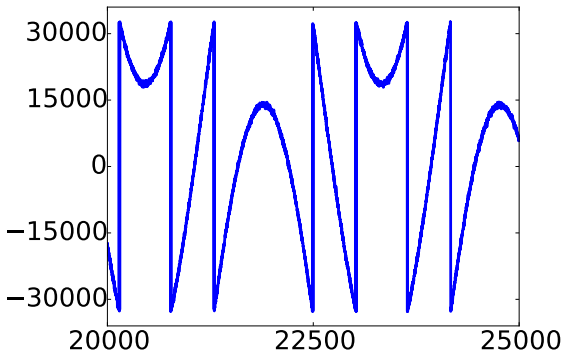
- Forced bitslip input
- Signal shaping analysis, 1st order derivative
- Autoscale trigger
- Guard time

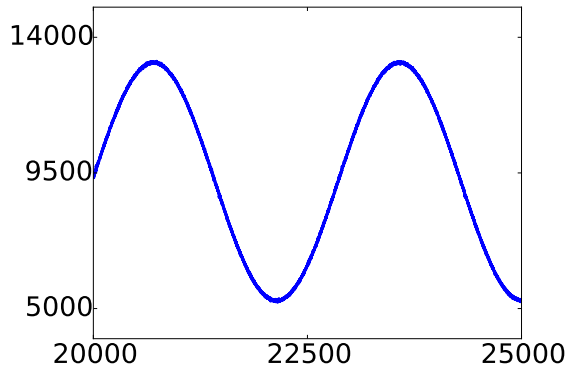
- Small FIFOs hardblocks near the IO

Syncronization and CDC (II)

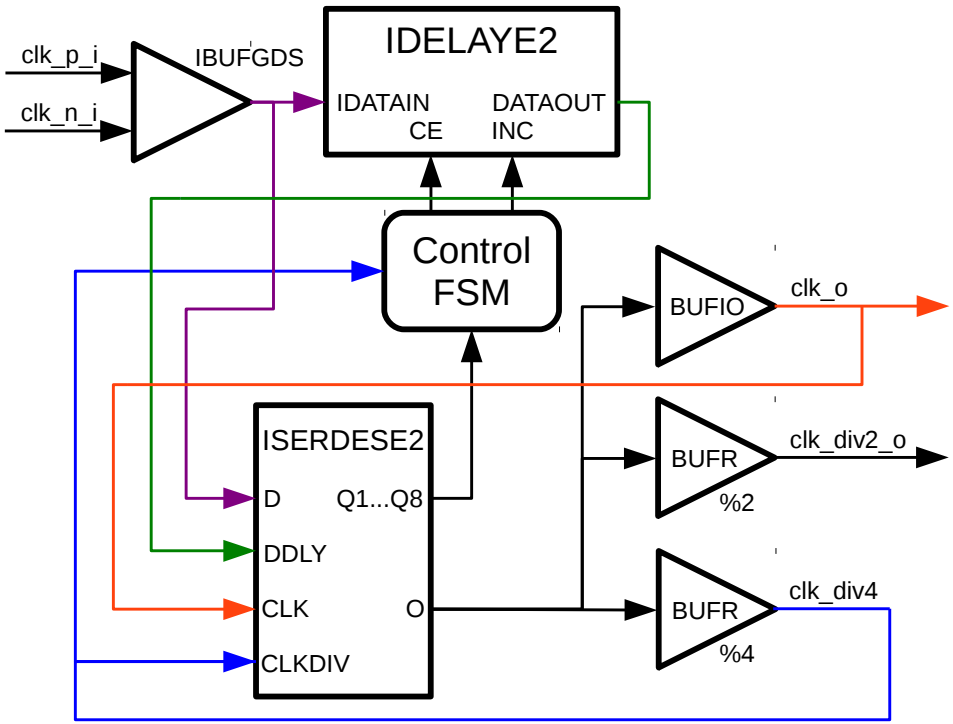








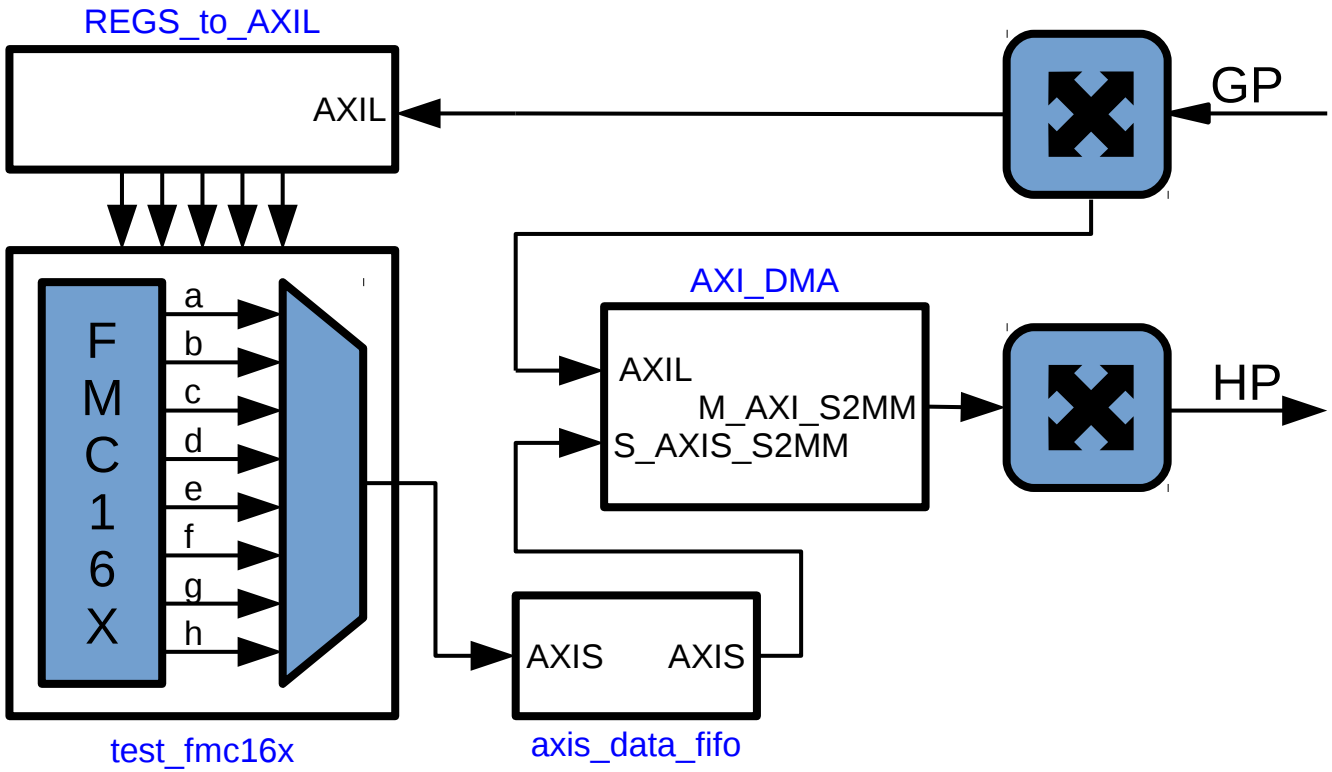
Clocking



Different frequencies operating in the system, 500MHz in the IO, 250MHz in data deserialization and 125MHz after the CDC.

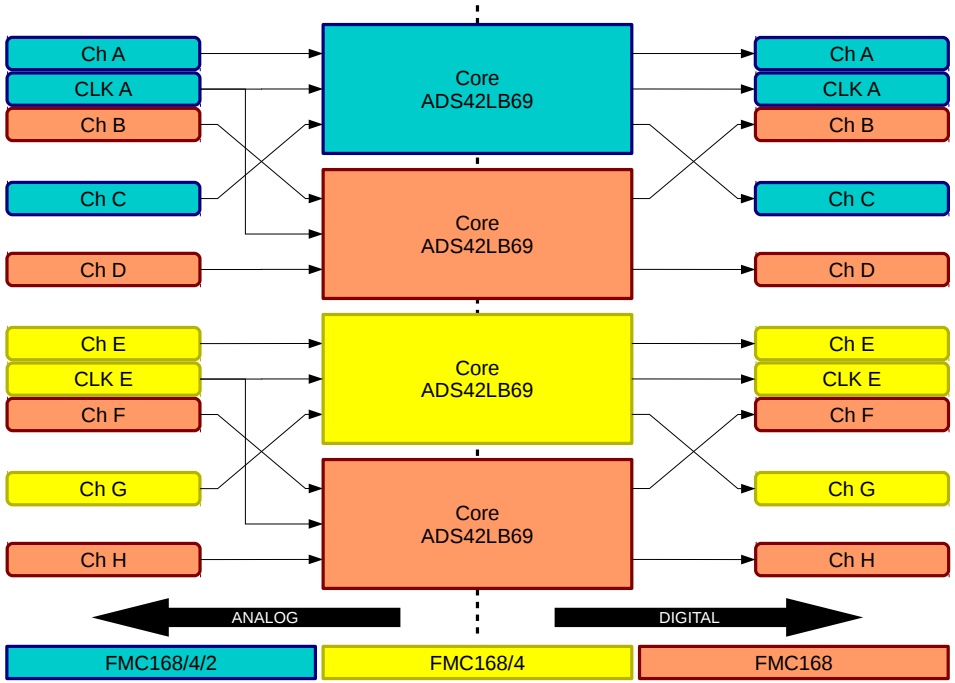
Outline

Design for testing the IP core



Top level

In order to be compatible with all the boards of the family, a set of generics are used enabling or disabling the resources by channels groups, depending on the board type.



Outline

Validation

- An internal fake data generator works muxed with SERDES to test the system, starting from the fifo's inputs.
- Python scripts to analyze the fake data.
- Fast Fourier Transform of a well known signal being sampled.

Outline

Conclusions

- QuADC
- Base for the FMC10X IP Core
- Packet Standardization

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INTI-CMNB-FPGA

Bruno Valinoti
valinoti@inti.gob.ar
bruno-valinoti

Rodrigo A. Melo
rmelo@inti.gob.ar
rodrigoalejandromelo
@rodrigomelo9ok
rodrigomelo9

Questions?

Thanks!