Open Repositories for FPGA development

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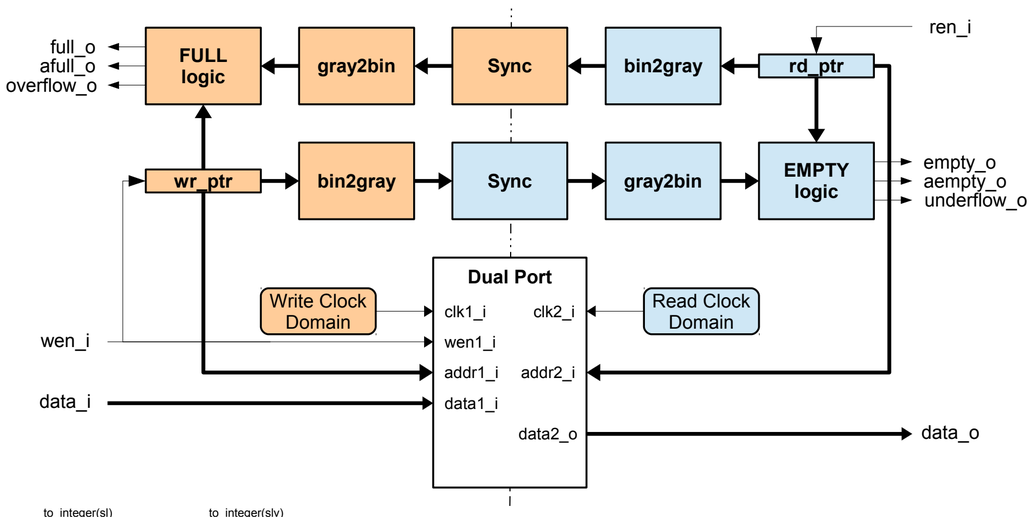
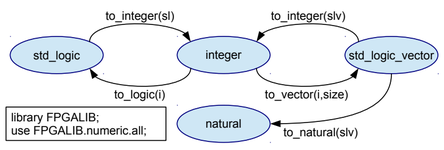
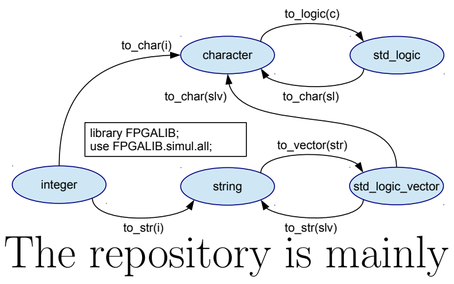
FPGA Lib (BSD 3-clause)







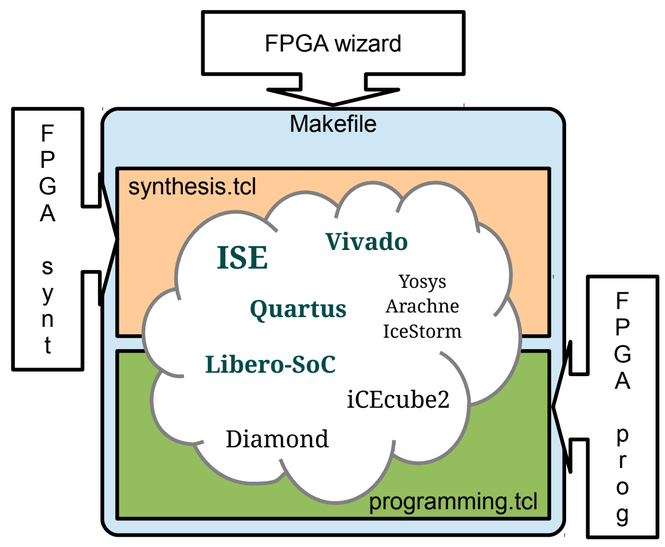
Library of HDL snippets (such as cores, procedures and functions) and small helper programs which are commonly shared between FPGA projects.

The repository is mainly composed by VHDL code, organized in five packages: **mems** (Simple, Dual and True Dual Port, and an A/Synchronous FIFO); **numeric** (type conversions and math operations); **simul** (utilities for testbenches); **sync** (to work with multiple clock domains); **verif** (to do simple and quick test in hardware).
Others components of the repository are small Python scripts, a Makefile to use with GHDL and some board pines definition.

vhdl2verilog (GPL3)

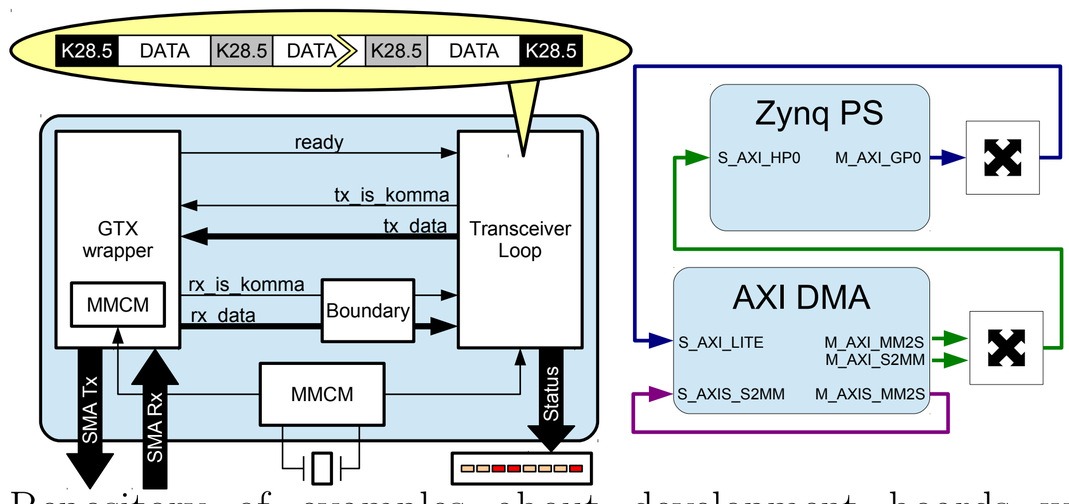
A free software compiler from synthesizable VHDL (93) to Verilog (2001). It will be used to convert the VHDL part of FPGA Lib to Verilog automatically but is developed with the aim of being useful to use in conjunction with other FOSS (*Free and Open Source Software*) for FPGAs, such as Yosys synthesis tool. It is developed using Flex and Bison.

FPGA Helpers (GPL3)



Development tools which simplify and unify the workflow between different manufacturers, allowing reproducibility and repeatability. Tool Command Language files for synthesis and programming, with a Makefile to abstract its execution. Python and Bash scripts, which help generate options files and execute the Tcl effectively for different tasks.

FPGA Examples (BSD 3-clause)



Repository of examples about development boards with FPGAs from Xilinx, Intel-Altera, Microsemi and Lattice. They are working and ready to test, allowing you to have a starting point for your own designs, with some of them including the use of advanced blocks of the device.

Repositories

FPGA Lib

FPGA Helpers

FPGA Examples

VHDL to Verilog