PROGRAM

WORKSHOPS

Lunes 27 de marzo 2023 / Monday 27th March 2023

Horario/ Time	Actividad / Activity
9 - 13 hs	**Workshop "Flow Design and Implementation for SoC-FPGA" C. Sisterna (UNSJ) & J. Dondo (UNSL) PART 1** **Coffee Break:** 10:30 – 11:00
13 - 14 hs	Almuerzo en comedor universitario / Lunch at University Cafeteria
14 - 18 hs	**Workshop "Flow Design and Implementation for SoC-FPGA" C. Sisterna (UNSJ) & J. Dondo (UNSL) PART 2** **Coffee Break:** 15:30 – 16:00

Martes 28 de marzo 2023 / Tuesday 28th March 2023

Horario/ Time	Actividad / Activity
9 - 13 hs	**Workshop: "FPGA-based Accelerated Cloud Computing using AMD-Xilinx Vitis" G. Sutter (Universidad Autónoma de Madrid) PART 1** **Coffee Break:** 10:30 – 11:00
13 - 14 hs	Almuerzo en comedor universitario / Lunch at University Cafeteria
14 - 18 hs	**Workshop "FPGA-based Accelerated Cloud Computing using AMD-Xilinx Vitis" G. Sutter (Universidad Autónoma de Madrid) PART 2** **Coffee Break:** 15:30 – 16:00

Miércoles 29 de marzo 2023 / Wednesday 29th March 2023

Horario/ Time	Actividad / Activity
9 - 13 hs	**Workshop: "Introduction to the Versal ACAP AI Engine and to its Programming Model" M. Ruiz (AMD Xilinx University Program) PART 1** **Coffee Break:** 10:30 – 11:00
13 - 14 hs	Almuerzo en comedor universitario / Lunch at University Cafeteria
14 - 18 hs	**Workshop: "Introduction to the Versal ACAP AI Engine and to its Programming Model" M. Ruiz (AMD Xilinx University Program) PART 2** **Coffee Break:** 15:30 – 16:00

CONFERENCIA / CONFERENCE

Jueves 30 de marzo 2023 / Thursday 30th March 2023

Horario / Time	Actividad / Activity
8 a 9 hs	Acreditación / Accreditation
9 hs	Apertura / Opening Ceremony
9.30 - 10:30	**Plenaria 1/ Keynote 1: AMD/Xilinx**
10:30 - 11:00	Coffee Break + Poster Session 1
11:00 - 11:20	"Hardware Acceleration of a CNN-based Automatic Modulation Classifier" Sravanth Chebrolu, Srinivas_Boppu and Linga Reddy Cenkeramaddi
11:20 - 11:40	"FPGA Implementation of Staggered Cellular Automata for Wave Propagation Simulation" Gustavo Pereira, Santiago Anaya, Henrique Moura and Daniel Muñoz
11:40 - 12:00	"Streamlining FPGA Circuit Design and Verification with Python and py4hw" David Castells-Rufas, Gemma Rotger and David Novo
12:00 - 13:00	**Plenaria 2 / Keynote 2: "FPGA prototyping for SoCs" Rodrigo A. Melo, Martin Heredia (indie Semiconductor)**
13:00 - 14:00	Almuerzo / Lunch
14:00 - 14:20	"Open- source SoC-FPGA Platform for Signal Processing" Matias Javier Oliva, Pablo Andres García, Enrique Spinelli and Alejandro Luis Veiga
14:20 - 14:40	"Multi-stage multirate filterbank for FPGA resource optimization" Luis Arnaldi
14:40 - 15:00	"Evaluation of dense and sparse linear algebra kernels in FPGAs" Federico Favaro, Ernesto Dufrechou, Juan Oliver and Pablo Ezzatti
15:00 - 15:40	**Invited Talk : *UVM framework state of the art"* Maia Desamo (Emtech)**
15:40 - 16:00	Coffee Break + Poster Session 2
16:00 - 16:40	**Invited Talk : *"Leveraging modern tools for higher productivity in FPGA development"* Nicolás Bértolo y José Ignacio Quinteros del Castillo (Emtech)**
16:40 - 17:00	"High-Speed Textural Image Features Extraction using FPGA" Jeremias Gaia, Emanuel Trabes, Eugenio Orosco, Gustavo Sutter, Francisco Rossomando and Carlos Miguel Soria
17:00 - 17:20	"Sphery vs. Shapes: A hardware-only raytraced game" Victor Suarez Rovere and Julian Kemmerer
17:20 - 18:20	**Plenaria 3/ Keynote 3: Synopsis**
21:30	Cena de camaradería / Fellowship dinner

Viernes 31 de marzo 2023 / Friday 31th March 2023

Horario / Time	Actividad / Activity
9:30 - 10:30	**Plenaria 4 /Keynote 4: "True random number generation with asynchronous circuits in FPGA" Andrés Cicuttin (ICTP)**
10:30 - 10:50	"Turbo-Código seguro mediante Interleaver aleatorio variable en el tiempo" Raúl Eduardo Lopresti, Jorge Castiñeira Moreira, Maximiliano Antonelli and Luciana De Micco
10:50 - 11:10	"Real-time noise reduction through independent channel averaging for real-time biomedical signal acquisition" Federico Guerrero, Matías Oliva and Enrique Spinelli
11:10 - 11:40	Coffee Break + Poster Session 3
11:40 - 12:00	"Diseño en VHDL del algoritmo SOGI PLL SRF usando síntesis de alto nivel (HLS)" Alejandro Enrique Nuñez Manquez, Martín Murdocca, Victor Yelpo and Ivana Trento
12:00 - 12:20	"Generador de fallas para pruebas de algoritmos de sincronización con la red eléctrica monofásica." Alejandro Enrique Nuñez Manquez, Julio Daniel Dondo Gazzano, Carlos Federico Sosa Paez and Estrella Gómez Orozco

12:20 - 12:40	“Acceleration of a Dense Monocular Localization System using FPGAs” Emanuel Trabes, Jeremias Gaia and Gustavo Sutter
13:00 - 14:00	Almuerzo / Lunch
14:00 - 15:00	**Plenaria remota de Marvell**
15:00 - 15:20	“SHA-3 Implementation for Post-Quantum Cryptography using High-Level Synthesis” Fernando Aparicio Urbano-Molano and Jaime Velasco-Medina
15:20- 16:00	“Remote Lab: an implementation guide and case study with free hardware boards” Astri Edith Andrada Tivani, Juan Ignacio Vergés, Julio Daniel Dondo Gazzano and Andrea Schwandt
16:00- 16:20	FPGA-Accelerated Convolutional Neural Network Mohammed Chelkha, Carlos Alberto Valderrama Sakuyama and Ali Ahaitouf
16:30	Acto de cierre y entrega de certificados / Closing ceremony
